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Datasheet for the decision of 23 February 2022

Case Number: T 2550/19 - 3.5.05

Application Number: 16200975.7

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IPC: G06F13/16

Language of the proceedings: EN

Title of invention:
MEMORY CONTROLLER WITH VIRTUAL CONTROLLER MODE

Applicant:
Advanced Micro Devices, Inc.

Headword:
Grouping memory access requests/AMD

Relevant legal provisions:
EPC Art. 56
RPBA Art. 12(2), 12(4)
RPBA 2020 Art. 12(3), 13(2)

Keyword:

Inventive step - (no)
Late-filed request - submitted with the statement of grounds of appeal - admitted (no)
Late-filed request - submitted during oral proceedings - admitted (no)

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Case Number: T 2550/19 - 3.5.05

D E C I S I O N
of Technical Board of Appeal 3.5.05
of 23 February 2022

Appellant: (Applicant)	Advanced Micro Devices, Inc. 2485 Augustine Drive Santa Clara, CA 95054 (US)
Representative:	Eve, Rosemary Margaret Venner Shipley LLP Windsor House 6-10 Mount Ephraim Road Tunbridge Wells, Kent TN1 1EE (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 20 March 2019 refusing European patent application No. 16200975.7 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chair	A. Ritzka
Members:	P. Tabery
	K. Kerber-Zubrzycka

Summary of Facts and Submissions

I. The appeal is directed against the examining division's decision to refuse the European patent application.

II. The examining division decided that the requirements of Article 56 and 123(2) EPC were not met by the application according to any of the requests.

III. The documents referred to by the examining division included:

D3 US 2006/294264 A1

IV. In its statement of grounds of appeal, the appellant requested that a patent be granted on the basis of the claims in accordance with either a main request or one of a first to third auxiliary requests, all of which were submitted with the statement of grounds of appeal.

V. The board issued a summons to oral proceedings. It also set out its preliminary opinion on the case (Article 15(1) RPBA 2020).

The board was of the opinion that the **main request** should be admitted into the proceedings, but that it did not meet the requirements of Article 56 EPC.

As for the **auxiliary requests**, the board indicated that it had to be discussed whether these requests should be admitted into the proceedings pursuant to Article 12(4) RPBA 2007.

VI. In its reply dated 23 January 2022, the appellant provided further arguments regarding the pending requests.

VII. Oral proceedings were held on 23 February 2022. The appellant requested that a patent be granted based on

the main request or on one of the first to third auxiliary requests, all of which had been filed with the statement of grounds of appeal dated 18 July 2019, or based on a fourth auxiliary request filed during the oral proceedings before the board.

VIII. **Claim 1** of the **main request** reads as follows:

"*A memory controller (500) having a memory channel controller (510), the memory channel controller (510) comprising:*

an address generator (522) for receiving memory access requests and decoding said memory access requests to select a rank and bank of memory devices in a memory system, and in a virtual controller mode further decoding a sub-channel number (612) of a plurality of sub-channels for each of said memory access requests;

a command queue (520) for storing decoded memory access requests including said sub-channel number (612) in said virtual controller mode; and

an arbiter (538) coupled to said command queue (520) to select memory access requests from said command queue (520) according to predetermined criteria, wherein in said virtual controller mode said arbiter (538) selects from among said memory access requests to pick eligible requests for each sub-channel independently using said predetermined criteria, and to provide said eligible requests to a dispatch queue (514);

said dispatch queue (514) providing memory commands to selected ones of a plurality of sub-channels (130/140)."

Independent **claim 12** reads as follows:

"*A method for controlling a memory system (120) having a plurality of memory channels (130/140), comprising:*

in a virtual controller mode:

receiving memory access requests;

decoding each of said memory access requests into a bank, a rank, and a sub-channel number corresponding to one of a plurality of sub-channels of memory devices in the memory system (120);

storing said decoded memory access request including said bank, said rank, and said sub-channel number in a command queue (520);

selecting from among a plurality of memory access requests in said command queue (520) using predetermined criteria, wherein said selecting further comprises selecting from among said memory access requests to each sub-channel independently using said predetermined criteria, providing selected memory access requests to a dispatch queue (514); and

dispatching said memory access requests, so selected, from said dispatch queue to one of the plurality of sub-channels according to said sub-channel number."

IX. Compared to the main request, it is further specified in **claim 1** of the **first auxiliary request** that the predetermined criteria of the arbiter in the virtual controller mode are those "*that it uses when virtual controller mode is not selected*".

X. **Claim 1** of the **second auxiliary request** differs from claim 1 of the main request in that it further specifies:

"*a set of configuration registers that store configuration information to determine how said address generator (522) decodes received address information, wherein the memory channel controller (510) uses only*

one set of configuration registers for the sub-channels".

XI. **Claim 1** of the **third auxiliary request** differs from claim 1 of the main request in that it further specifies:

"*wherein said arbiter (538) staggers the issuance of commands between the individual sub-channels.*"

XII. **Claim 1** of the **fourth auxiliary request** differs from claim 1 of the main request in that it further specifies:

"*wherein said dispatch queue (514) comprises:*

a selector (620) having an input for receiving a decoded memory access provided by said command queue (520), a first output, and a second output, and selecting between said first and second outputs based on said sub-channel number (612);

a first queue (630) having an input coupled to said first output of said selector (620), a bidirectional port for connection to a physical interface, PHY, of a first sub-channel, and a set of entries each of which stores a decoded memory access request; and

a second queue (640) having an input coupled to said second output of said selector (620), a bidirectional port for connection to a physical interface, PHY, of a first sub-channel, and a set of entries each of which stores a decoded memory access request."

Reasons for the Decision

1. The application concerns increasing the efficiency of modem DDR memory controllers. Grouping memory access requests that relate to the same row in a given rank of memory avoids the overhead of activating another row.

2. Main request

2.1 Admissibility (Article 12(4) RPBA 2007)

Claim 1 of the main request differs from claim 1 of the fifth auxiliary request considered in the impugned decision in that the feature relating to the sending of requests by the arbiter has been replaced by a feature relating to a dispatch queue providing the requests.

The appellant submitted that this amendment overcame the examining division's objection relating to added subject-matter (Article 123(2) EPC).

The board holds that the amended claims meet the requirements of Article 123(2) EPC. Furthermore, the objection based on Article 84 EPC has been rendered moot. Therefore, the main request constitutes a reaction to the objections raised in the impugned decision. Thus, the board has decided to admit the main request into the proceedings.

2.2 Novelty (Article 54(1) EPC)

The board holds that document **D3** discloses the following features of **claim 1** (the references in parentheses relate to that document; strike-through is used to indicate features it does not disclose):

A memory controller having a memory channel controller, the memory channel controller comprising:
("memory control component 110 includes two memory controllers 112 (memory controllers 1 and 2), one for each of the two channels", see [0019] and Fig. 2*)*

(i) an address generator for receiving memory access requests and decoding said memory access requests ~~to select a rank and bank of memory devices in a memory system~~, and ~~in a virtual controller mode further~~ decoding a sub-channel number of a plurality of sub-channels for each of said memory access requests; *("Identity Subchannel Assignment",* see [0023]*)*

(ii) a command queue for storing decoded memory access requests including said sub-channel number ~~in said virtual controller mode~~; and *("Reorder buffer 220 collects requests to enable transaction assembler 230 to attempt to assemble memory accesses for each memory 240 subchannel",* see [0022]*)*

(iii) an arbiter coupled to said command queue to select memory access requests from said command queue according to predetermined criteria, wherein ~~in said virtual controller mode~~ said arbiter selects from among said memory access requests to pick eligible requests for each sub-channel ~~independently~~ using said predetermined criteria, and to provide said eligible requests ~~to a dispatch queue~~ *("The memory controller forms a memory read transaction by selecting S read requests, one for each subchannel, from the reorder buffer 220", "The portion of the address represented by shared address lines is the same for all subchannel requests in the transaction",* see [0024]*)*;

(iv) ~~said dispatch queue~~ providing memory commands to selected ones of a plurality of sub-channels *("... a memory read transaction ... for each subchannel",* see [0024]*)*.

Hence, the differences between the subject-matter of **claim 1** and that of document **D3** reside in that:

A) a rank and bank of memory devices are selected (when decoding memory requests);

B) the memory controller provides two different modes;

C) eligible requests for each sub-channel are picked independently using said predetermined criteria;

D) memory requests (commands) are sent through a dispatch queue.

The subject-matter of **claim 1** is therefore novel over the disclosure in document **D3**.

2.3 Inventive step (Article 56 EPC)

The board considers that differences A) to D) are directed to different problems and do not interact synergistically, i.e. they may be implemented independently of one another. They thus constitute a juxtaposition rather than a true combination of features. Thus, to prove that the aggregation of distinguishing features does not involve an inventive step it is sufficient to show that the individual distinguishing features are obvious.

2.3.1 Difference A)

Difference A) achieves the technical effect that targeted locations in memory may be accessed. The technical problem may therefore be regarded as being how targeted memory locations can be accessed. The board concurs with the examining division that organising memory in ranks and banks is part of the skilled person's common knowledge. The decoding of requests therefore inherently includes the decoding of those organisation units. In view of this, difference A) does not solve a technical problem in a non-obvious manner.

2.3.2 Difference B)

The board notes that document **D3** mentions in paragraph [0016] that "*the memory efficiency of memory device supporting both a graphics system and a CPU is limited*

since memory access size for graphics is often ideally 4 to 16 bytes, while memory architectures are optimized for the 64 byte CPU line size to optimize CPU memory efficiency." This passage hints to the skilled person that the objective technical problem is "*how to allow for efficient memory access by both a CPU and a graphics controller*". To solve this problem, the skilled person would ensure that the memory controller also supports a "*normal*" memory access mode (being more efficient for the CPU's memory access), in addition to the memory access mode using sub-channels. In this way, the skilled person would arrive at difference B) without having to employ any inventive skill.

2.3.3 Difference C)

The board concurs with the appellant and interprets this difference as relating to the "*predetermined criteria*" being applied independently to each request when picking the eligible requests. Since the term "*independently*" allows for a broad interpretation, it is not, however, excluded that the "*predetermined criteria*" are those criteria already known from document **D3**. The board considers that no technical effect can be derived from applying the known criteria "*independently*". In the absence of a technical effect which is plausibly caused by difference C), this difference cannot contribute to an inventive step.

2.3.4 Difference D)

The board notes that a queue is a commonly known data structure for storing objects in sequence for later retrieval. Hence, the technical effect caused by difference D) is that the eligible requests are stored in sequence until needed again. On the basis of what is commonly known, the skilled person would provide another queue, should the need arise. In this way, the skilled person would arrive at difference D) without

having to employ any inventive skill. Therefore, difference D) cannot contribute to an inventive step.

2.3.5 Consequently, the board considers that the subject-matter of **claim 1** is not inventive over the disclosure in document **D3**.

2.3.6 The appellant argued that document **D3** was concerned with splitting a memory channel, whereas the claimed invention related to different whole channels, albeit with the same term, "*sub-channel*", being used. Therefore, the requests could be "*picked independently*", which was not the case in the disclosure in document **D3**. As described in the application as originally filed, see paragraph [0040] and Fig. 6, the sub-channel number was only used in the presence of several physical sub-channels (virtual controller mode). On the other hand, in the case of a single sub-channel, sub-channel numbers were not used (normal mode). Therefore, the technical problem solved by the invention related to *"how to design memory controllers to be flexible enough to be configured for different memory types, including types that support sub-channels"* (see the appellant's letter dated 23 January 2022).

2.3.7 The board notes that the term "*independently*" as used in claim 1 might point in the direction of independent channels. However, the board considers that this term allows for a broad interpretation, such that no technical effect can be derived therefrom. As to the other alleged differences brought forward by the appellant, the board holds that these are not reflected in the wording of claim 1. Furthermore, the board is not convinced by the technical problem presented by the appellant. The board considers this technical problem to be overly ambitious and not credibly solved by difference C), nor any of the other identified

differences. Therefore, the appellant's argumentation has failed to convince the board.

2.4 In view of the above, the **main request** is not allowable.

3. First auxiliary request

The appellant argued that the "*predetermined criteria*" were now defined in claim 1. Furthermore, document **D3** did not disclose such criteria.

The board notes that the amendment now defines that the predetermined criteria are notably not related to sub-channels. The board thus concurs with the appellant that the amended feature is novel over the disclosure in document **D3**. However, the board considers that the predetermined criteria may also comprise the timing of activate commands, which the application as originally filed explains as being caused by the properties of DRAM ("*DRAM has a minimum specified time between activate commands to the same bank, known as* t_{RC}", see paragraph [0036]). Thus, the timing of activate commands is a commonly known property of DRAM which the skilled person would have taken into account when putting into practice what is disclosed in document **D3**. Therefore, the skilled person would have arrived at the amended feature without having to employ any inventive skill. For this reason, the amended feature cannot contribute to an inventive step. Since the amended feature does not interact synergistically with the remaining distinguishing features, and since these were also found to be obvious (see the reasoning provided with respect to claim 1 of the main request), the board holds that the subject-matter of claim 1 of the first auxiliary request is not inventive over the disclosure in document **D3**.

In view of the above, the **first auxiliary request** is not allowable.

4. Second auxiliary request

The appellant argued that document **D3** disclosed the duplication of resources with two different memory controllers. Hence, there would be no incentive for the skilled person to adapt this solution to provide a *single* set of configuration registers, as claimed in claim 1. Therefore, the amended feature rendered the subject-matter of claim 1 inventive over the disclosure of document **D3**.

The board notes that the term "*set of configuration registers*" does not limit the number of configuration registers. The amended feature thus allows for an interpretation that comprises what is disclosed in document **D3**. Therefore, the distinguishing features of claim 1 of the second auxiliary request are the same as those of claim 1 of the main request. Consequently, claim 1 of the second auxiliary request is not inventive over the disclosure of document **D3** for the same reasons as for claim 1 of the main request.

In view of the above, the **second auxiliary request** is not allowable.

5. Third auxiliary request

The board notes that the feature added to claim 1 ("*staggering*") was examined in the impugned decision in the context of the third auxiliary request. In the impugned decision, the examining division concluded that the amended feature was not inventive as it was "*equivalent to interleaving or pipelining which may effect shorter time delays*". This was "*considered as*

common knowledge" and known *"since the 1970s*". The board asserts that the appellant did not explain, in the statement of grounds of appeal, why the considerations of the examining division might be incorrect. Hence, the board holds that the appellant did not fully plead its case with respect to the third auxiliary request.

The appellant argued that the respective line of argument had been provided in its letter dated 23 January 2022.

The board notes that Article 12(2) RPBA 2007 (which is equivalent to Article 12(3) RPBA 2020) requires that the statement of grounds of appeal "*shall set out clearly and concisely the reasons why it is requested that the decision under appeal be reversed*". The appellant did not comply with this requirement since the respective line of argument was not contained in the statement of grounds of appeal; rather, it was only provided in response to the board's preliminary opinion.

In view of the above, the board has decided not to admit the third auxiliary request into the proceedings (Article 12(4) RPBA 2007 refers back to Article 12(2) RPBA 2007, which is thus deemed applicable although not explicitly mentioned in the transitional provisions of Article 25(2) RPBA 2020).

6. Fourth auxiliary request

Claim 1 of the fourth auxiliary request is a combination of claim 1 of the main request and the features of dependent claim 3 of the main request.

The appellant argued that notably by defining separate physical interfaces, claim 1 was clearly distinguished from the disclosure of document **D3**. Furthermore, the

amendments were based on a dependent claim and were submitted in reaction to the board's conclusion regarding the main request. Therefore, the fourth auxiliary request should be admitted into the proceedings.

The board considers that since no arguments regarding the respective dependent claim 3 were provided in the statement of grounds of appeal, this combination with a dependent claim constitutes an amendment to the appellant's case. The board notes that Article 13(2) RPBA 2020 requires "*exceptional circumstances, which have been justified with cogent reasons*" for the admittance of an amendment to a party's appeal case at the oral proceedings before the board.

The appellant further argued that this amendment was a reaction to the broad interpretation of the claim's wording by the board at the oral proceedings.

However, the board holds that this broad interpretation was already contained in the impugned decision. Therefore, the board concludes that no such exceptional circumstances exist. Consequently, the board has decided not to admit the fourth auxiliary request into the proceedings (Article 13(2) RPBA 2020).

7. In view of the above, the appeal is not allowable.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chair:

K. Götz-Wein A. Ritzka

Decision electronically authenticated