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**Datasheet for the decision of 1 February 2024**

**Case Number:** T 0610/20 - 3.4.03

**Application Number:** 11741318.7

**Publication Number:** 2596521

**IPC:** H01L21/24, H01L21/04, H01L29/24, H01L29/861, H01L21/3213, H01L21/329

**Language of the proceedings:** EN

**Title of invention:**
ELECTRONIC DEVICE STRUCTURE INCLUDING A BUFFER LAYER ON A BASE LAYER

**Applicant:**
Wolfspeed, Inc.

**Relevant legal provisions:**
EPC Art. 123(2)
RPBA 2020 Art. 12(2), 12(4), 12(6), 13(2)

**Keyword:**
Main request - not admitted under Art. 12(4) and (6) RPBA
Auxiliary requests 1 to 3 - not admitted under Art. 13(2) RPBA as in force from 1 January 2024

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**Case Number: T 0610/20 - 3.4.03**

# D E C I S I O N
# of Technical Board of Appeal 3.4.03
# of 1 February 2024

| | |
|---|---|
| **Appellant:** (Applicant) | Wolfspeed, Inc.<br>4600 Silicon Drive<br>Durham, NC 27703 (US) |
| **Representative:** | FRKelly<br>Waterways House<br>Grand Canal Quay<br>Dublin D02 PD39 (IE) |
| **Decision under appeal:** | **Decision of the Examining Division of the European Patent Office posted on 30 October 2019 refusing European patent application No. 11741318.7 pursuant to Article 97(2) EPC.** |

**Composition of the Board:**

| | |
|---|---|
| **Chairman** | T. Häusser |
| **Members:** | M. Ley |
| | G. Decker |

## Summary of Facts and Submissions

I. The appeal is against the decision of the examining division to refuse European patent application No. 11 741 318 pursuant to Article 97(2) EPC.

II. The examining division decided *inter alia* that claim 1 according to the main request and the auxiliary request then on file did not meet the requirements of Article 123(2) EPC.

III. With its statement of grounds of appeal, the appellant filed amended claims according to a new main request which aimed at overcoming the objections raised by the examining division.

IV. The board issued a communication under Article 15(1) RPBA and set out its preliminary opinion that the amended claims *inter alia* did not overcome the objections under Article 123(2) EPC raised by the examining division and gave rise to additional objections *inter alia* under Article 123(2) EPC. For this reason, the board was not minded to admit the claims of the main request into the appeal proceedings under Article 12(4) RPBA.

V. By letter dated 2 January 2024, the appellant replied to the board's communication and submitted arguments why the claims according to the main request "properly [overcame] all the objections pending against the application".

VI. With a letter dated 31 January 2024, i.e. one day before the oral proceedings, the appellant filed amended claims according to auxiliary requests 1 to 3.

VII. At the oral proceedings before the board the appellant requested that the decision under appeal be set aside and that a European patent be granted on the basis of the claims according to the main request filed with the statement setting out the grounds of appeal, or alternatively according to one of auxiliary requests 1 to 3 filed with the letter dated 31 January 2024.

VIII. Claim 1 according to the main request has the following wording:

*A semiconductor wafer having a plurality of electronic devices formed thereon, where each electronic device of the plurality of electronic devices includes a plurality of layers comprising:*

*a semiconductor base layer (80) of a first doping type;*

*a semiconductor buffer layer (82) of the first doping type on the semiconductor base layer;*

*one or more contact layers (84, 86) of a second doping type opposite the first doping type on the semiconductor buffer layer that form a first contact region of the electronic device;*

*a highly doped well (88) of the first doping type in the semiconductor base layer that forms a second contact region of the electronic device; and*

*a semiconductor ledge layer (94) of the second doping type on a sidewall of the one or more contact layers and a surface of one of the semiconductor buffer layer and the semiconductor base layer,*
*wherein the semiconductor buffer layer and the semiconductor ledge layer are doped such that when the semiconductor ledge layer is provided on the semiconductor buffer layer, a depletion region (96) is formed in the semiconductor buffer layer between the highly doped well and the one or more contact layers.*

Claim 1 according to auxiliary request 1 has the following wording:

*A semiconductor wafer having a plurality of gate turn-off thyristors, GTOs, formed thereon, where each GTO of the plurality of GTOs includes a plurality of layers comprising:*

*a semiconductor base layer (80) of a first doping type;*

*a semiconductor buffer layer (82) of the first doping type on the semiconductor base layer (80), the buffer layer (82) having a doping level less than or equal to $1x10^{17}$ carrier [sic] per $cm^3$;*

*one or more contact layers (84, 86) of a second doping type opposite the first doping type on the semiconductor buffer layer (82) that form a first contact region of the GTO;*

*a highly doped well (88) of the first doping type in the semiconductor base layer (80) that forms a second contact region of the GTO, the highly doped well having a doping level greater than or equal to $1x10^{18}$ carrier [sic] per $cm^3$; and*

*wherein each GTO near the center of the semiconductor wafer includes an epitaxially grown semiconductor ledge layer (94) of the second doping type on a sidewall of the one or more contact layers (84, 86) and a surface of the semiconductor buffer layer (82) and the semiconductor base layer (80), the ledge layer (94) having a doping level less than or equal to $1x10^{17}$ carrier [sic] per $cm^3$ and composed of the same semiconductor material as the base layer (80), buffer layer (82) and contact layers (84, 86), wherein the semiconductor buffer layer (82) and the semiconductor ledge layer (94) create a depleted region (96);*

*wherein each GTO near the outer edge of the semiconductor wafer includes the epitaxially grown semiconductor ledge layer (94) on a sidewall of the one or more contact layers (84, 86) and a surface of the semiconductor base layer (80).*

Claim 1 according to auxiliary request 2 has the following wording:

*A method of fabricating a plurality of gate turn-off thyristors, GTOs on a semiconductor wafer, the method comprising:*

*providing a semiconductor buffer layer (82) on a semiconductor base layer (80), the semiconductor buffer layer (82) and the semiconductor base layer having a first doping type, and the buffer layer (82) having a doping level less than or equal to $1x10^{17}$ carrier [sic] per $cm^3$;*

*providing one or more contact layers (84, 86) on the semiconductor buffer layer (82), the one or more contact layers (84, 86) being of a second doping type that is opposite the first doping type;*

*etching the one or more contact layers (84, 86) to form a first contact region for each one of the plurality of GTO;*

*providing a highly doped well (88) of the first doping type in the semiconductor base layer (80) that forms a second contact region of the GTO, the highly doped well having a doping level greater than or equal to $1x10^{18}$ carrier [sic] per $cm^3$; and*

*providing, when an amount of over-etch when etching the one or more contact layers (84, 86) to form the first contact region is less than the thickness of the semiconductor buffer layer (82), an epitaxially grown semiconductor ledge layer (94) of the second type on a sidewall of the one or more contact layers (84, 86) and*

*a surface of the semiconductor buffer layer (82) and the semiconductor base layer (80), the ledge layer (94) having a doping level less than or equal to 1x10$^{17}$ carrier [sic] per cm$^{3}$ and composed of the same semiconductor material as the base layer (80), buffer layer (82) and contact layers (84, 86), wherein the semiconductor buffer layer (82) and the semiconductor ledge layer (94) create a depletion region (96);*

*providing, when an amount of over-etch when etching the one or more contact layers (84, 86) to form the first contact region is greater than or equal to the thickness of the semiconductor buffer layer (82), the epitaxially grown semiconductor ledge layer (94) on a sidewall of the one or more contact layers (84, 86) and a surface of the semiconductor base layer (80).*

Claim 1 according to auxiliary request 3 has the following wording:

*A method of fabricating a plurality of gate turn-off thyristors, GTOs on a semiconductor wafer, the method comprising:*

*providing a semiconductor buffer layer (82) on a semiconductor base layer (80), the semiconductor buffer layer (82) and the semiconductor base layer (80) having a first doping type, the semiconductor base layer (80) having a doping level in the range of 1x10$^{16}$ to 1x10$^{17}$ carrier [sic] per cm$^{3}$ and the buffer layer (82) having a doping level in the range of 1x10$^{17}$ to 1x10$^{18}$ carrier [sic] per cm$^{3}$;*

*providing one or more contact layers (84, 86) on the semiconductor buffer layer (82), the one or more contact layers (84, 86) being of a second doping type that is opposite the first doping type;*

*etching the one or more contact layers (84, 86) to form a first contact region for each one of the*

*plurality of GTO wherein the thickness of the semiconductor buffer layer (82) is equal to a maximum amount of over-etch on the semiconductor wafer when etching the one or more contact layers (84, 86) to form the first contact region;*

*providing a highly doped well (88) of the first doping type in the semiconductor base layer (80) that forms a second contact region of the GTO, the highly doped well having a doping level greater than or equal to 1x10$^{18}$ carrier [sic] per cm$^{3}$; and*

*providing, when the amount of over-etch when etching the one or more contact layers (84, 86) to form the first contact region is less than the thickness of the semiconductor buffer layer (82), an epitaxially grown semiconductor ledge layer (94) of the second type on a sidewall of the one or more contact layers (84, 86) and a surface of the semiconductor buffer layer (82) and the semiconductor base layer (80), the ledge layer (94) having the same doping level as the buffer layer (82) and composed of the same semiconductor material as the base layer (80), buffer layer (82) and contact layers (84, 86), wherein the semiconductor buffer layer (82) and the semiconductor ledge layer (94) create a depletion region (96);*

*providing, when an amount of over-etch when etching the one or more contact layers (84, 86) to form the first contact region is equal to the thickness of the semiconductor buffer layer (82), the epitaxially grown semiconductor ledge layer (94) on a sidewall of the one or more contact layers (84, 86) and a surface of the semiconductor base layer (80).*

IX. The appellant argued that the main request and auxiliary requests 1 to 3 should be admitted into the appeal proceedings.

## Reasons for the Decision

1. The invention as disclosed in the application

The invention relates to an electronic device structure that includes a buffer layer to compensate for non-uniform etching over a semiconductor wafer and to protect the semiconductor surface of the electronic device.

Figures 1A, 1B, 2 and 3 disclose a conventional process of manufacturing silicon carbide gate turn-off thyristors (GTOs). A number of semiconductor layers 14 to 22 is provided. P-type semiconductor layers 20 and 22 are etched down to N-type base layer 18 so that they form an anode of the GTO. As a result of the etching process, there is substantial damage to the crystalline structure both at sidewall surfaces 24 of the P-type semiconductor layers 20, 22 and at a surface 26 of the N-type base layer 18. This damage results in interface charge, surface traps and surface recombination, which decreases the gain of the top transistor (formed of layers 16, 18, 20) of the GTO and results in an instability of the turn-on current and in an increase of the on-resistance of the GTO.

Another issue that arises during fabrication is non-uniform etching. When etching the P-type semiconductor layers 20 and 22 via Reactive Ion Etching (RIE) or a similar etching process, etching occurs faster near the edge of the semiconductor wafer than at the center of the semiconductor wafer, which results in over-etching of the GTOs near the edge of the semiconductor wafer into their N-type base layers 18, as illustrated in Figures 2 and 3. As a result, said

GTOs near the edge of the semiconductor wafer fail to operate, which reduces the production yield.

Both issues were addressed by an additional buffer layer for reducing damage to the semiconductor base layer, wherein a thickness of the semiconductor buffer layer compensates for over-etch. The thickness of the P-type buffer layer is equal to the maximum amount of over-etch or larger, said amount being a function of both the type of etching and a position of the GTO on the semiconductor wafer. In this case, as shown in Figures 4C, 5 to 7, 8D, 9 to 11, surface recombination is mitigated or eliminated and the GTOs at the wafer's edge are operable.

As claimed, a semiconductor ledge layer is provided on a sidewall of the contact layers and a surface of either the semiconductor buffer layer or the semiconductor base layer, see Figures 8D, 9 to 11. This semiconductor ledger layer mitigates or eliminates interface charge and reduces surface recombination.

2. Main request - admittance under Article 12(4) and (6) RPBA

2.1 Article 12(2) RPBA stipulates that, in view of the primary object of the appeal proceedings to review the decision under appeal in a judicial manner, a party's appeal case shall be directed to the requests, facts, objections, arguments and evidence on which the decision under appeal was based.

According to Article 12(4) RPBA, any part of a party's appeal case which does not meet the requirements in paragraph 2 is to be regarded as an amendment, unless the party demonstrates that this part was admissibly

raised and maintained in the proceedings leading to the decision under appeal. Any such amendment may be admitted only at the discretion of the board.

The board shall exercise its discretion in view of, *inter alia*, the complexity of the amendment, the suitability of the amendment to address the issues which led to the decision under appeal, and the need for procedural economy.

Furthermore, the board shall not admit requests, facts, objections or evidence which should have been submitted, or which were no longer maintained, in the proceedings leading to the decision under appeal, unless the circumstances of the appeal case justify their admittance, see Article 12(6) RPBA.

2.2 In the present case, the examining division referred to claims 7, 8, 28 and 29, Figures 8D and 10, and paragraphs [0043] and [0044] as originally filed and held that a doped semiconductor ledge layer according to the invention was disclosed only in combination with the following features (see the reasons of the decision under appeal, points 1.1 and 1.1.1):

(a) said semiconductor ledge layer being of the second doping type,
(b) said semiconductor ledge layer being disposed on a surface of the semiconductor buffer layer only if the amount of over-etch is less than the thickness of the semiconductor buffer layer, and being otherwise disposed on the surface of the semiconductor base layer,
(c) the semiconductor buffer layer being lightly doped,
(d) the semiconductor buffer layer being of the first doping type,

(e) the semiconductor ledge layer being of the same semiconductor material as base, buffer and contact layers,
(f) the semiconductor ledge layer being lightly doped,
(g) the semiconductor ledge layer being epitaxially grown.

2.3 In the statement setting out the grounds of appeal, the appellant argued that the claims had been extensively amended to overcome the examining division's objections under Article 123(2) EPC. As a basis for the amendments made to claim 1, the appellant indicated figures 8A to 8D as well as paragraphs [0038], [0041], [0043] and [0044] as originally filed. As a basis for the newly added claims 12 to 17, it indicated paragraphs [0037], [0043] and claims 7 and 11 as originally filed.

In its letter dated 2 January 2024, the appellant essentially indicated paragraphs [0007], [0008], [0023] and [0055] as a justification for omitting features (c), (e) and (f) in claim 1. Said paragraphs made it clear that devices other than the GTO of figure 8D were possible. During oral proceedings before the board, the appellant also argued that it had the impression that it was not necessary to attend the oral proceedings before the examining division.

2.4 It is undisputed that the claim set according to the main request is an amendment of the appellant's case under Article 12(2) and (4) RPBA.

In its communication pursuant to Article 15(1) RPBA , the board preliminarily agreed with the examining division that claim 1 did not meet the requirements of Article 123(2) EPC. The board also raised additional

objections under Article 123(2) EPC against features introduced into claim 1 for the first time with the statement setting out the grounds of appeal.

The board accepts that the appellant addressed the omission of features (a) and (d) listed in point 2.2 above by specifying the doping types of the semiconductor ledge and buffer layers and addressed feature (b) by the arguments provided in the paragraph bridging pages 1 and 2 of the statement setting out the grounds of appeal. However, the appellant did not provide any arguments why the omission of features (c) and (e) to (g) was justified under Article 123(2) EPC, nor did it amend the claims accordingly. With respect to paragraphs [0007], [0008], [0023] and [0055] indicated in the appellant's letter dated 2 January 2024, the board notes that they were not discussed in the statement setting out the grounds of appeal.

It is thus clear for the board that the set of amended claims filed with the statement of the grounds of appeal is not suitable to address the issues which led to the decision under appeal.

2.5 Moreover, the appellant submitted the set of claims underlying the impugned decision one month prior to the oral proceedings before the examining division and announced that it would not attend the oral proceedings. With a brief communication, as an additional service in examination proceedings, the examining division informed the appellant that the date fixed for oral proceedings was maintained. This means that there were objections still outstanding that needed to be discussed at the oral proceedings. Consequently, the appellant should have expected that

problems relating to the requests filed in reply to the summons to oral proceedings would be dealt with at the oral proceedings. The board is not aware of any facts that could have given the impression to the appellant that its presence during oral proceedings before the examining division was not necessary. Hence, the claims according to the main request filed with the statement of grounds of appeal could and should have been submitted already during the oral proceedings before the examining division to address the examining division's objections.

2.6 In view of these considerations, the board decided not to admit the main request into the appeal proceedings under Article 12(4) and (6) RPBA.

3. Auxiliary requests 1 to 3 - admittance under Article 13(2) RPBA (as in force from 1 January 2024)

According to Article 13(2) RPBA as in force from 1 January 2024, any amendment to a party's appeal case made after notification of a communication under Article 15, paragraph 1, shall, in principle, not be taken into account unless there are exceptional circumstances, which have been justified with cogent reasons by the party concerned.

In the present case, the board issued its communication under Article 15(1) RPBA 2020 on 4 April 2023. The set of claims according to auxiliary requests 1 to 3 were filed on 31 January 2024, i.e. on the day prior to the oral proceedings before the board.

Neither in its short letter dated 31 January 2024 nor during oral proceedings before the board did the appellant present cogent reasons to justify that there

were exceptional circumstances for filing the new requests at this very late stage of the proceedings. It merely expressed its hope that the board would exercise its discretion to admit auxiliary requests 1 to 3 into the appeal proceedings.

The board is not aware of any exceptional circumstances justified by cogent reasons that would justify the filing of auxiliary requests 1 to 3 to address the issues raised by the examining division at this very late stage of the proceedings. Indeed, the appellant could and should have filed the new requests already in the first-instance proceedings or, at the very latest, with its statement of grounds of appeal. Thus, the board decided not to admit auxiliary requests 1 to 3 into the appeal proceedings under Article 13(2) RPBA as in force from 1 January 2024.

4. In the absence of any admissible request, the appeal must fail.

**Order**

**For these reasons it is decided that:**

The appeal is dismissed.

The Registrar: The Chairman:

S. Sánchez Chiquero T. Häusser

Decision electronically authenticated