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Datasheet for the decision of 3 June 2022

Case Number: T 1478/20 - 3.5.05

Application Number: 13777457.6

Publication Number: 2917842

IPC: G06F13/16, G06F13/28

Language of the proceedings: EN

Title of invention:
INTELLIGENT DUAL DATA RATE (DDR) MEMORY CONTROLLER

Applicant:
Qualcomm Incorporated

Headword:
INTELLIGENT MEMORY CONTROLLER / Qualcomm

Relevant legal provisions:
EPC Art. 123(2)
RPBA 2020 Art. 13(1)

Keyword:
Amendment to appeal case - amendment gives rise to new objections (yes)
Amendments - allowable (no) - added subject-matter (yes)

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Case Number: T 1478/20 - 3.5.05

D E C I S I O N
of Technical Board of Appeal 3.5.05
of 3 June 2022

Appellant: (Applicant)	Qualcomm Incorporated 5775 Morehouse Drive San Diego, CA 92121 (US)
Representative:	Bardehle Pagenberg Partnerschaft mbB Patentanwälte Rechtsanwälte Prinzregentenplatz 7 81675 München (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 19 December 2019 refusing European patent application No. 13777457.6 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chair	A. Ritzka
Members:	N. H. Uhlmann
	E. Mille

Summary of Facts and Submissions

I. The applicant appealed against the decision of the examining division to refuse the European patent application in suit.

II. The examining division decided that neither the subject-matter of the independent claims of the main request nor that of auxiliary requests 1 and 2 involved an inventive step.

III. The examining division made reference to, *inter alia*, the following documents:

D1 US 6 529 968
D2 US 2005/210163
D3 EP 1 396 792.

IV. With its statement setting out the grounds of appeal, the appellant maintained the requests underlying the contested decision.

V. The board summoned the appellant to oral proceedings.

In a communication under Article 15(1) RPBA 2020, the board set out its provisional opinion on the case.

VI. With a letter dated 2 May 2022, the appellant submitted a new main request and renamed the previous requests auxiliary requests 1 to 3.

VII. The oral proceedings took place via videoconference.

VIII. The appellant's final requests were that the decision under appeal be set aside and that a patent be granted on the basis of the set of claims of the main request filed with the appellant's letter dated 2 May 2022, or, alternatively, on the basis of one of auxiliary requests 1 to 3 (originally designated the main request

and auxiliary requests 1 and 2) filed with the appellant's letter dated 24 November 2019.

IX. Claim 1 of the main request is worded as follows:

"A method of transferring data from a first memory under control of a first memory controller to a second memory under control of a second memory controller, comprising:

receiving (402) a source address and a destination address at the first memory controller configured to perform a data transfer operation between the first memory under control of the first memory controller and the second memory, under control of the second memory controller, using the system bus only once;

determining (404), by the first memory controller, whether the source address is in the first memory;

determining (408), by the first memory controller, whether the destination address is in the first memory; and

when the first memory controller determines that the source address is in the first memory and the destination address is not in the first memory:

retrieving (412), by the first memory controller, the data stored at the source address; and

sending (414), by the first memory controller, a write command, the destination address and the data stored at the source address to the second memory controller using the system bus only once."

X. Claim 1 of auxiliary request 1 is worded as follows:

"A method of transferring data to and from one or more memories, comprising:

receiving (402) a source address and a destination address in a first memory controller that includes a master controller module, the master controller module included in the first memory controller configured to perform at least one direct memory access operation to effect at least one memory-to-memory data transfer operation between a first memory under control of the first memory controller and a second memory, under control of a second memory controller, using the system bus only once;

determining (404) in the first memory controller whether the source address is in the first memory;

determining (408) in the first memory controller whether the destination address is in the first memory;

sending (414) by the first memory controller a write command, the destination address and data stored at the source address to the second memory controller using the system bus only once when the first memory controller determines that the source address is in the first memory and the destination address is not in the first memory."

XI. Claim 1 of auxiliary request 2 is based on claim 1 of auxiliary request 1 and specifies the following further step:

"pushing the data stored at the source address and the destination address onto the bus in response to determining that the source address is in the first memory and the destination address is not in the first memory."

XII. Claim 1 of auxiliary request 3 is based on claim 1 of auxiliary request 2 and specifies the following further two steps:

"pushing a read request, the source address, and the destination address on to the bus in response to determining that the source address is not in the memory; and

copying the data stored at the source address to the destination address without pushing any data onto a bus when the memory controller determines that both the source address and the destination address are in the memory."

Reasons for the Decision

1. The present application pertains to a method for transferring data between memories. A memory controller includes a master controller module. When the transfer is to take place between two memories connected to different memory controllers, the controller responsible for the source memory sends the data to be copied and the destination address to the controller responsible for the target memory.

Main request

2. Admittance, Article 13(1) RPBA

2.1 The amended claim 1 does, *prima facie*, give rise to an objection under Article 123(2) EPC. The reasons for this are set out in the following.

2.2 The independent method claim 1 was amended after the board issued its preliminary opinion under Article 15(1) RPBA. The appellant stated that the amendments were based on Figure 4 and paragraphs 55 to 58 of the description.

2.3 Claim 1 as amended refers to a first and a second memory controller but does not refer to a direct memory access controller or to a master component/controller.

2.4 All claims as filed and as amended in the course of the first-instance proceedings refer to a direct memory access controller. The description (e.g. paragraphs 2 to 10 in the summary section, and paragraphs 29, 39, 40, 42 to 45, 50, 53 and 54 in the detailed description) also clearly teaches that a direct memory access controller (or a master component/controller, see paragraphs 29 and 39) is an essential feature of the invention.

The only parts of the application which do not explicitly refer to either a direct memory access controller or a master component/controller are Figures 4 and 5 and paragraphs 55 to 62. However, paragraphs 55 and 59 refer to memory controller 206, which according to Figures 2 and 3 includes a master controller module.

Consequently, there is no basis for deleting a direct memory access controller from the claims.

2.5 The appellant stated that paragraphs 55 and 59 referred to memory controller 206 by way of example only.

The board is not convinced by this argument. It is true that the formulation "e.g." is used in these paragraphs, but the application does not include any teaching or example showing that the invention could be performed without a direct memory access controller.

2.6 Hence, the criteria in Article 13(1) RPBA that amendments must not give rise to new objections is not satisfied and therefore the main request is not admitted into the proceedings.

Auxiliary request 1

3. Amendments

The board holds that the claims do not meet the requirements of Article 123(2) EPC.

3.1 The appellant argued that the amended claims were based on paragraphs 40 to 46, 50 and 58 of the description and Figures 2 to 5.

3.2 No basis is apparent for **the master controller module** being configured to perform at least one direct memory access operation to effect at least one memory-to-memory data transfer operation between a first memory, under control of the first memory controller, and a second memory, under control of a second memory controller, using the system bus only once.

The description sets out four specific cases regarding the master controller module:

- Both the source address and the destination address identify locations outside the first memory (paragraphs 43 and 54). This case is excluded by the language of the claim.

- Both the source address and the destination addresses identify locations inside the first memory (paragraphs 44 and 53). This case is similarly excluded by the language of the claim.

- The source address identifies a location inside the first memory and the destination address references a location outside of the first memory (paragraph 45). This case falls under the wording of the claim. However, paragraph 45 additionally states that the source address identifies a location inside the first memory and that data is retrieved from the source address and sent, together with the

destination address, to the second memory controller via the bus. No basis is apparent for omitting these further features with regard to the master controller module.

- The master controller module may be configured to allow a direct memory access controller to perform the memory transfer operations (paragraph 54). This case is excluded by the language of the claim, i.e. "using the system bus only once".

3.3 Consequently, auxiliary request 1 is not allowable.

Auxiliary requests 2 and 3

4. Amendments

The objections set out above with regard to auxiliary request 1 (see section 3. above) also apply to auxiliary requests 2 and 3.

Hence, these auxiliary requests are not allowable either.

5. Conclusion

None of the requests on file meets the requirements of the EPC. Thus, the appeal is not allowable.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chair:

K. Götz-Wein A. Ritzka

Decision electronically authenticated