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Datasheet for the decision of 21 March 2022

Case Number: T 1862/20 - 3.5.03

Application Number: 12849857.3

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Language of the proceedings: EN

Title of invention:
Reducing the effect of non-linear kick-back in switched capacitor networks

Applicant:
Analog Devices, Inc.

Headword:
Dealing with kick-back errors/ANALOG DEVICES

Relevant legal provisions:
EPC Art. 56, 84

Keyword:
Clarity - main request (yes)
Inventive step - main request (yes)

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Case Number: T 1862/20 - 3.5.03

D E C I S I O N
of Technical Board of Appeal 3.5.03
of 21 March 2022

Appellant: (Applicant)	Analog Devices, Inc. One Analog Way Wilmington, MA 01887 (US)
Representative:	Horler, Philip John Withers & Rogers LLP 2 London Bridge London SE1 9RA (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 17 April 2020 refusing European patent application No. 12849857.3 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chair	K. Bengi-Akyürek
Members:	R. Gerdes
	F. Bostedt

Summary of Facts and Submissions

I. The examining division refused the present patent application on the grounds that the claims of the main request and the first to third auxiliary requests were not clear (Article 84 EPC) and that the subject-matter of the independent claims of these requests was not new (Article 54 EPC) or did not involve an inventive step (Article 56 EPC). The decision relied on the following documents:

D12: S.C. Lee et al.: "Digital Calibration of Nonlinear Memory Errors in Sigma-Delta Modulators", IEEE Transactions on Circuits and Systems 1: Regular Papers, vol. 57, no. 9, 1 September 2010 (2010-09-01), pp. 2462-2475;

D13: J.P. Keane et al.: "Digital background calibration for memory effects in pipelined analog-to-digital converters", IEEE Transactions on Circuits and Systems 1: Regular Papers, vol. 53, no. 3, 1 March 2006 (2006-03-01), pp. 511-525.

II. The applicant (appellant) appealed against this decision and requested that the decision under appeal be set aside and that a patent be granted on the basis of one of the **main or first and second auxiliary requests** submitted with the statement setting out the grounds of appeal. The claims of the main request were identical to those of the third auxiliary request of the decision under appeal.

III. **Claim 1** of the main request reads as follows (with a numbering of features by the board):

"A method, comprising:

(a) injecting (312) a randomly determined amount of dither into a digital-to-analog converter (DAC) component in a first stage (100) of a multi-stage pipelined analog-to-digital converter (ADC), the DAC having a switched capacitor network comprising a plurality of capacitors (8C) that are switchably connected to an input signal source to the ADC, wherein the dither is injected by:

(b) connecting a first capacitor (CCal) to a first or second reference voltage (Vref+, Vref-) in accordance with a randomly generated number (RN) when the switched capacitor network is disconnected from the input signal source during a hold phase of the switched capacitor network, and

(c) connecting the first capacitor in parallel with the capacitors of the switched capacitor network when the switched capacitor network is connected to the input signal source to sample an input signal (Vin+, Vin-) during a subsequent sampling phase of the switched capacitor network, such that in the presence of kickback between the switched capacitor network and the input signal source, at least some charge from the first capacitor is sampled by the switched capacitor network with the input signal at the end of the subsequent sampling phase;

(d) after injecting the dither, determining (316) at least one gain coefficient (GC) by correlating the random number (RN) and an overall digital output of the ADC corresponding to the input signal sampled during the subsequent sampling phase, wherein the gain coefficient is indicative of a transfer function of the kick-back;

(e) generating (320), as a function of the at least one gain coefficient, the random number (RN) and a digital output of the first stage (D1)

corresponding to a previous input sample, at least two correction values corresponding to a contribution of the kick-back to the overall digital output of the ADC; and

(f) subtracting (320) the correction values from the overall digital output of the ADC, thereby correcting for kick-back errors in the overall digital output."

IV. Independent **claim 3** of the main request reads (with a numbering of features adapted to that of claim 1):

"A multi-stage pipelined analog-to-digital converter (ADC), comprising:

(a) a hardware arrangement that injects a randomly determined amount of dither into a digital-to-analog (DAC) component in a first stage (100) of the multi-stage ADC, the DAC having a switched capacitor network comprising a plurality of capacitors (8C) that are switchably connected to an input signal source to the ADC, the hardware arrangement configured to inject the dither by:

(b) connecting a first capacitor (CCal) to a first or second reference voltage (Vref+, Vref-) in accordance with a randomly generated number (RN) when the switched capacitor network is disconnected from the input signal source during a hold phase of the switched capacitor network, and

(c) connecting the first capacitor in parallel with the capacitors of the switched capacitor network when the switched capacitor network is connected to the input signal source to sample an input signal (Vin+, Vin-) during a subsequent sampling phase of the switched capacitor network, such that in the presence of kickback between the switched capacitor network and the input signal source, at

least some charge from the first capacitor is sampled by the switched capacitor network with the input signal at the end of the subsequent sampling phase;

(d) a correlation circuit that, after the dither is injected, determines at least one gain coefficient (GC) by correlating the random number (RN) and an overall digital output of the ADC corresponding to the input signal sampled during the subsequent sampling phase, wherein the gain coefficient is indicative of a transfer function of the kick-back; and

(e) a correction circuit that generates, as a function of the at least one gain coefficient, the random number (RN) and a digital output of the first stage (D1) corresponding to a previous input sample, at least two correction values corresponding to a contribution of the kick-back to the overall digital output of the ADC, and

(f) subtracts the correction values from the overall digital output of the ADC, thereby correcting for kick-back errors in the overall digital output."

Reasons for the Decision

1. The present application

The application concerns a method for reducing "kick-back noise" in a multi-stage pipelined analog-to-digital converter (ADC). Capacitors of a switched capacitor network are connected to an input signal source during a *sample* phase, then switched to reference voltage sources during a *hold (amplify)* phase. Depending on the sampling frequency and input source characteristics, residual charge stored in the

capacitors can become superimposed onto the value of the input signal source when the capacitors are switched to the input signal source during the next sample phase. Part of this "kick-back" can be sampled by the input network at the end of this next sampling phase, which can cause distortion of the sampled signal, memory effects and performance degradation (see paragraphs [0002] to [0009] of the application as published). The application proposes estimation of the effects of kick-back noise by injecting a random dither signal into the first stage of the ADC (see Fig. 4).

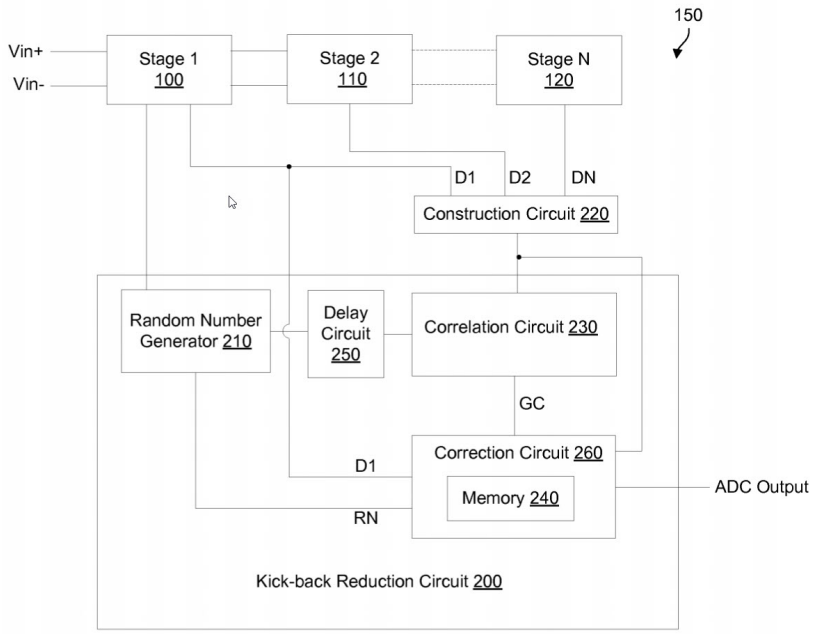

Fig. 4

For the purpose of injecting the dither signal, the application uses an extra capacitor, which is charged according to the random dither signal in the hold phase of the ADC and is connected to the input voltage in the sample phase. The method generates the digital output signal as a combination of the output signals of the multiple stages of the pipelined ADC ("overall digital output", see step 316 of Fig. 7 and paragraph [0042]).

This output signal of the ADC represents the digitised input signal including errors resulting from kick-back noise. According to the application, the overall digital output is correlated with the known dither signal in order to estimate the effect of kick-back noise from the dither signal on the output signal. By repeating the correlation for each (or every nth) input sample, an approximation of the gain coefficient of the kick-back noise is calculated (see paragraphs [0042] to [0049]). On the basis of this gain coefficient, the contributions of kick-back noise from the dither signal (KB1) and the previous input sample (KB2) on the overall digital output can be calculated. By subtracting these contributions from the digitised output signal, a corrected ADC output signal can be calculated (see paragraphs [0050] to [0053]).

2. *Main request, clarity - Article 84 EPC*

2.1 The examining division held in the decision under appeal that claim 1 of the then third auxiliary request, which corresponds to the present main request, was not clear (see Reasons 4.1 of the decision). The expression "such that in the presence of kickback between the switched capacitor network and the input signal source, at least some charge from the first capacitor is sampled by the switched capacitor network with the input signal at the end of the subsequent sampling phase" used in feature (c) gave the impression that the dither injection process was performed in some particular way that guaranteed that its charge was at the same time affecting the input signal source and was sampled by the switched capacitor network. In practice, the way in which the dither injection was performed had nothing to do with how much of the currently injected dither leaked into the next signal sample due to

incomplete settling of the sampling process caused by excessive load from the switched capacitor network and/or insufficient drive from the input signal source. Therefore, the skilled reader would not know which technical features the applicant was referring to (Article 84 EPC), for instance in case the switched capacitor network settled to the final value with sufficient accuracy within the given sampling clock period. This was because, in that case, none of the embodiments described throughout the application would leak the dither or part of the dither onto the input signal regardless of what type of dither injection process was used.

2.2 The board agrees that the amount of kick-back noise is dependent on the drive capability (output impedance) of the input source and the load presented by the switched capacitor network. Hence, depending on the input signal source, there may be cases in which the switched capacitor network settles to the final value with sufficient accuracy. However, it is incorrect that the way in which the dither injection is performed has nothing to do with how much of the currently injected dither leaks into the next signal sample. For example, the timing of "connecting the first capacitor in parallel with the capacitors of the switched capacitor network" has in fact an influence on the amount of charge injected into the switched capacitor network.

The allegedly unclear feature defines that some charge from the first capacitor contributes to the sampled input signal under the condition that there is "kickback between the switched capacitor network and the input signal source". It specifies that the previous input signal and the charge from the first capacitor contribute in a similar manner to kick-back

noise if there is any. In other words, feature (c) is a functional feature which limits the claim in the sense that the circuitry and timing must be such that - if there is kick-back - then the charge from the first capacitor is at least partially present in the next sample. The functional feature therefore implies certain restrictions on the circuitry and timing of the dither injection which are partially redundant in view of the previous feature (c), i.e. "connecting the first capacitor in parallel with the capacitors of the switched capacitor network when the switched capacitor network is connected to the input signal source to sample an input signal (Vin+, Vin-) during a subsequent sampling phase of the switched capacitor network". However, the feature implies further restrictions. It excludes embodiments which do not result in a charge from the first capacitor being sampled by the switched capacitor network if at the same time a charge from the previous sampling phase of the switched capacitor network affects the sampled input voltage.

2.3 Therefore, the board considers the disputed feature to be clear. Furthermore, the board is satisfied that the remainder of claim 1 as well as the further claims of the main request also comply with Article 84 EPC.

3. Main request, inventive step - Article 56 EPC

3.1 It is undisputed that document **D13** can be considered the closest prior art with respect to the claimed subject-matter. Similar to the present application, D13 is concerned with the calibration of a pipelined ADC using a dither signal (see the section titled "Calibration Using DAC Dithering and Stage Redundancy", pages 519 to 522). The aim is to compensate for memory errors that can occur at all stages of a pipelined ADC.

These memory errors are caused by internal effects in the ADC such as capacitor dielectric absorption/ relaxation. However, the internal error sources have the same effect as the kick-back noise, i.e. some charge from the previous sample is transferred to the subsequent signal sample.

According to D13, a random digital signal is added to the input signal of the DAC of the first stage of the pipelined ADC. It adds redundancy to the pipeline stages "using more ADSC and DASC levels than would be necessary". This means that some additional capacitors may be added to the switched capacitor network, but these capacitors are operated in the same way as the other capacitors, i.e. connected to the reference voltages in accordance with the output signal of the ADSC augmented by the dither value r_i during the hold phase (see figure 9). Document D13 also discloses that the dither signal is correlated with the digital output value to determine a gain coefficient (i.e. equation (63)). The calibration in D13 is carried out recursively (stage-by-stage starting with the last one) (see equation (73) and page 522, left-hand column) or according to equations (96) and (53). The latter equations compute the weighting factors of the individual stages based on the DASC gain K_i and the estimated inter-stage gain $\hat{M}_j$ corresponding to the gain coefficients.

3.2 Hence, compared to present claim 1, D13 does not disclose the use of a dedicated capacitor for the dither injection as specified in features (b) and (c). In addition, D13 does not disclose the use of the overall digital output value for determining the gain coefficient according to feature (d), nor does it disclose the generation of two correction values that

are subtracted from the digital output value according to features (e) and (f).

3.3 The examining division argued in the decision under appeal that a correlation of "the random number and an overall digital output of the ADC" according to feature (d) was disclosed in D13, equation (89). However, as argued by the appellant, equation (89) is only a step of the proof towards obtaining the update expressions (92) and (93), and not a step of the calibration method itself. A correlation of the random number r_i and a digital output $\hat{x}_i$ is disclosed in equation (63), but this correlation is applied to each stage individually, i.e. it does not use the overall digital output value. With respect to features (e) and (f), the examining division referred to equation (93) together with the following sentence, and page 517, left-hand column, lines 2 to 6. However, equation (93) only defines an update equation for the gain coefficient estimate, whereas the following passage only generally refers to the use of digital filters for removal of errors from memory effects ("memory errors").

3.4 Hence, claim 1 is distinguished from the disclosure of D13 by features (b) to (f). These features have the technical effect of performing background calibration of a pipelined ADC in view of errors arising from the transfer of residual charge from a previous to the subsequent signal sample. The objective problem formulated in the appealed decision (i.e. providing an "alternative method of injecting dither into a first stage of a multi-stage pipelined analog-to-digital converter in order to remove the memory errors") only results from the effects of distinguishing features (b) and (c). An objective technical problem taking all

distinguishing features into account is rather to be formulated as *how to adapt the calibration of D13 in view of further types of residual charge errors*.

3.5 Starting from **D13** and faced with the above objective technical problem, it is questionable whether the skilled person in the field of electronics would have even considered kick-back errors in the context of the underlying scheme. This is because, firstly, D13 does not mention this kind of error and, secondly, a sample&hold-amplifier is used, as shown in figure 1 of D13, that already suppresses kick-back errors.

Nevertheless, even if kick-back errors were considered by the skilled person, it would not be obvious to adapt the teaching of D13 to these specific errors. Nor does the decision under appeal demonstrate such an adaptation, which would require departing from the recursive approach used in D13 and from a correlation of the overall digital output value with the respective random dither signal.

3.6 Document **D12** discloses the use of a dedicated capacitor for dither injection (see page 2647, last paragraph). However, there is no information about the adaptation of the calibration algorithm to the presence of kick-back noise. The other documents on file also do not disclose such an algorithm.

3.7 Hence, having regard to the available prior art, the subject-matter of claim 1 and the corresponding apparatus claim 3 involves an inventive step (Article 56 EPC).

4. In conclusion, given that the objections against the main request (that corresponds to the third auxiliary

request underlying the decision under appeal) are not maintained, a patent can be granted on the basis of the claims of the present main request.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the examining division with the order to grant a patent on the basis of claims 1 to 5 of the main request, as filed with the statement setting out the grounds of appeal, and with a description and drawings to be adapted thereto.

The Registrar: The Chair:

B. Brückner K. Bengi-Akyürek

Decision electronically authenticated