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Datasheet for the decision of 7 October 2025

Case Number: T 0064/23 - 3.4.03

Application Number: 19167097.5

Publication Number: 3525237

IPC: H01L25/065, H01L25/07, H01L25/18, H01L27/14, H01L27/146, H04N5/369

Language of the proceedings: EN

Title of invention:
SEMICONDUCTOR DEVICE, SOLID-STATE IMAGE SENSOR AND CAMERA SYSTEM

Applicant:
Sony Group Corporation

Headword:

Relevant legal provisions:
EPC Art. 52(1), 56, 84, 123(2)

Keyword:
Claims - support in the description (yes)
Amendments - allowable (yes)
Inventive step - after amendment - (yes)

Decisions cited:
T 0438/22, T 0095/23

Catchword:

Europäisches Patentamt
European Patent Office
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Beschwerdekammern

Boards of Appeal

Chambres de recours

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Case Number: T 0064/23 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 7 October 2025

Appellant: (Applicant)	Sony Group Corporation 1-7-1 Konan Minato-ku Tokyo 108-0075 (JP)
Representative:	Müller Hoffmann & Partner Patentanwälte mbB St.-Martin-Straße 58 81541 München (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 25 July 2022 refusing European patent application No. 19167097.5 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	T. Häusser
Members:	A. Böhm-Pélissier
	T. Bokor

Summary of Facts and Submissions

I. The appeal is directed against the decision of the examining division refusing European patent application No. 19 167 097 for lack of inventive step (Articles 52(1) and 56 EPC) referring to the communications dated 7 January 2022 and 12 July 2021.

II. Reference is made to the following documents:

D1: WO 2006/129762
D1a: US 2010/0276572 A1
(US application corresponding to D1)
D2: US 2006/0220673 A1
D3: US 7,129,985 B1
D4: US 2005/0035381 A1

III. At the end of the oral proceedings before the board the appellant (applicant) **requested** that the decision of the examining division be set aside and that a patent be granted on the basis of the following documents:

—

Description:
pages 1-5, 5a, 5b, filed on 12 December 2019,
pages 6 to 28 as originally filed,

Claims:
no. 1 to 4 filed during oral proceedings before the board on 7 October 2025, titled "auxiliary request 2",

Drawings:
sheets 1/22 to 22/22 as originally filed.

IV. **Claim 1** according to the **sole request** titled "Auxiliary Request 2" (feature labelling "(A)", "(B)" etc. and

highlighting of amendments with respect to claim 1 underlying the impugned decision added by the board):

(A) A solid-state image sensor (10) comprising:
(B) a first chip (11), wherein the first chip (11) is a CMOS image sensor, CIS, chip; and
(C) a second chip (12), wherein
(D) the first chip (11) and the second chip (12) are bonded to have a stacked structure,
(E) the first chip (11) includes a pixel array unit (101) in which a number of pixels containing photoelectric conversion elements are arranged two-dimensionally in a matrix, and
(F) a high-voltage transistor circuit,
(G) the second chip (12) includes a low-voltage transistor circuit having lower breakdown voltage than the high-voltage transistor circuit, and
(H) the first chip (11) and the second chip (12) are connected by through contact vias (120), TCVs formed as through holes from ~~in~~ the first chip (11) to a wiring layer of the second chip (12) and being filled with metal.

V. The arguments of the appellant as far as they are essential for this decision can be summarised as follows:

(a) The claims of the sole request meet the requirements of Articles 84 and 123(2) EPC.

(b) The combination of features of claim 1 of the sole request is not obvious over the teachings of D1 to D4.

Reasons for the Decision

1. The invention

The invention concerns imaging devices typically assembled as modules with two separate chips: a CMOS image sensor (CIS) chip and an image processor chip (IPC), either mounted on individual packages or using a chip-on-board (COB) method. However, recent demands for reduced mounting areas and smaller sizes for devices like mobile phones have led to the development of System on Chip (SOC) technology, integrating both chips on a single chip. Despite its size advantage, SOC integration faces challenges, including increased manufacturing complexity, higher costs, and difficulty balancing analogue and logic characteristics, which can degrade device performance. To address these limitations, alternative methods for assembling the chips at the chip level are proposed, aiming to both minimize size and enhance performance (description of the application, paragraphs [0002] to [0004]).

As an alternative to the SOC and COB technologies, the invention proposes a stacked chip solution, i.e. a stack of CIS and IPC mounted one on top of the other and interconnected by bondings and vias wherein the chips are driven at different voltages.

2. Articles 123(2) and 84 EPC

2.1 Article 123(2) EPC

2.1.1 On the basis of section [0025] (highlighting added by the board) of the originally filed description, the

features underlined in section IV. were added to feature (H):

[0025] ... The first chip (upper chip 11) is patterned, and then through holes are formed from the first chip 11 to a wiring layer of the second chip (lower chip) 12 and filled with metal to form vias. In the embodiment, the vias are referred to as TCVs.

2.1.2 Section [0025] describes the concept of stacked chips in very general terms using the schematic drawing in Figure 3 and in contrast to the concept of the first and second chips on one and the same substrate, which is shown in Figure 2.

2.1.3 Other features described in connection with Figure 3, such as the formation of the wafer and the attachment of signal lines, are technically independent of how the through holes are formed. Consequently, the features underlined above can be isolated from the context of the description and of the context of Figure 3 without any unallowable intermediate generalisation.

Furthermore, from the originally filed drawings and the description as a whole, it is clear to the skilled person that, in the given context, the "through contact vias" in claim 1 are formed as through holes. Therefore, the board holds that this clarification of the unclear feature "TCV" on the basis of the description is not an unallowable amendment. It is directly and unambiguously apparent to the skilled person when reading the application as a whole.

2.1.4 Consequently, claim 1 of the sole request meets the requirements of Article 123(2) EPC.

2.2 Article 84 EPC

As a result of the clarifications described above, claims 1 to 4 also meet the requirements of Article 84 EPC. The board notes that the description, pages 1 to 28, is not in contradiction with the subject-matter defined in the new claims (T 0438/22, catchword, item 1) and also meets the requirements of Rule 42(1)(b) EPC (discussion of relevant prior art).

3. Inventive step

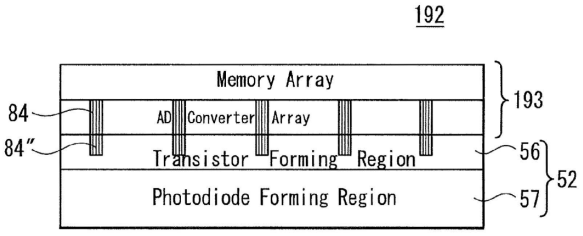
3.1 Closest state of the art

3.1.1 The examining division considered documents D3 and D4 as most suitable starting points for the problem and solution approach. However, D3 does not disclose a chip stack and D4 discloses neither different voltages in the first and second chips, nor transistors in the first chip (sensor chip).

3.1.2 The board considers that D1 (references are to the corresponding application D1a) not only discloses a chip stack comprising a first and a second chip according to claim 1, but also that different voltages in the first chip and in the second chip are intrinsic, since specific low voltage ranges are disclosed for the second chip. Consequently, D1 is considered to be the closest state of the art.

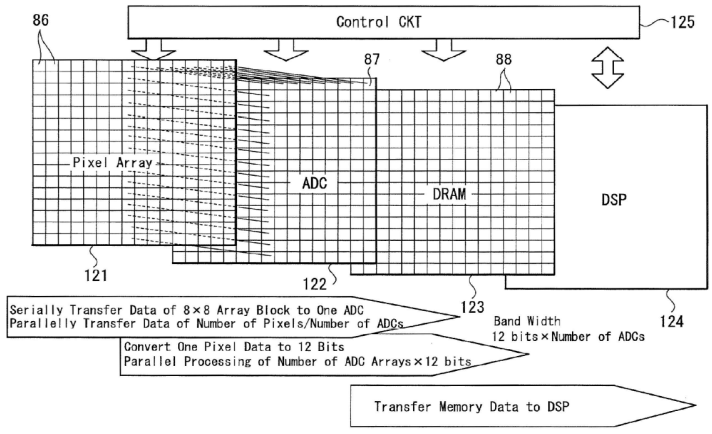
3.2 Document D1/D1a

FIG. 31B



D1a

FIG. 5



D1a

3.2.1 D1/D1a discloses a stack of two chips:

(i) A CCD driver chip 56 that controls photodiode pixels 57. The wafer substrates 56 and 57 can be considered to be the first chip (see D1a, Figure 31B).

(ii) The chip 193, which comprises the A/D converter array and the memory array, is considered the second chip (D1a, Fig. 31B).

3.2.2 The top of the first chip is thermally bonded to the bottom of the second chip. D1a discloses in Figure 9 that the memory array is operated in a voltage range of approximately one volt. A low operating voltage range inevitably implies a low breakdown voltage range. Therefore, the breakdown voltages of parts of the second chip in D1a are in the low voltage range of breakdown voltages.

3.2.3 D1a does not explicitly disclose the breakdown voltage of the driver circuit 56 or the range in which the photodiodes are operated.

3.2.4 Claim 1 defines "through contact vias" ("TCVs") that are formed as through-holes from the first chip to a wiring layer of the second chip and filled with metal.

3.2.5 The expression "through contact vias" as such is considered to be a broad term covering any vertical contact in the substrate, as it is not a term commonly used and known in the field of semiconductor technology, contrary to terms like "through holes", "through vias", "through silicon vias" or "through via contact". A "through contact" or a via may also be a blind via or buried via that does not pass through the entire substrate, such as the "through contact via" 84'' in figure 31B, which is formed in the first chip.

3.2.6 During the oral proceedings before the board the appellant clarified feature (H) in that it was specified that the expression "through contact vias" refers to through-holes that penetrate the entire first chip. The "through contact vias" 84'' of D1/D1a cannot be regarded as through-holes, as they are blind vias.

3.3 **Disclosure of D1/D1a**

3.3.1 D1/D1a therefore discloses (references to D1a, wording of claim 1)

(A) a solid-state image sensor comprising:
(B) a first chip (52), wherein the first chip is a CMOS image sensor (CCD image sensor), CIS, chip; and
(C) a second chip (processing chip 193), wherein

(D) the first chip and the second chip are bonded to have a stacked structure (Figure 31B),
(E) the first chip includes a pixel array unit (pixels in the "Photodiode Forming Region") in which a number of pixels containing photoelectric conversion elements (photodiodes) are arranged two-dimensionally in a matrix (array),
(F) and a ~~high-voltage~~ transistor circuit (56),
(G) the second chip includes a low-voltage transistor circuit (memory array) having low~~er~~ breakdown voltage ~~than the high-voltage transistor circuit~~, and
(H) the first chip and the second chip are connected by through contact vias (84'' in Figure 31B), TCVs, ~~formed as through holes from the first chip to a wiring layer of the second chip~~ and being filled with metal.

3.3.2 Consequently, D1 fails to disclose

(a) that parts of the first chip are driven at higher voltages than parts of the second chip;

(b) that the first chip comprises through vias extending through the whole chip.

3.4 Technical effect of the differences and objective technical problem to be solved

3.4.1 Feature (a) has the technical effect of reducing noise, i.e. increasing noise immunity, in particular 1/f noise and clock noise (see description of the application, paragraphs [0007], [0011] and [0018]; D3, column 7, lines 52 to 55; D2, paragraph [0007]).

3.4.2 Feature (b) has the technical effect of increasing flexibility in circuit design, so that power supply and contacting of any parts of the circuits in the second

chip are possible by means of contacts through the first chip (vias). Consequently, sequential processing of the data is also possible, for example.

3.4.3 The objective technical problem to be solved is to achieve these effects.

3.5 Non-obviousness

ad (a)

3.5.1 The board considers it obvious that the sensor chip is operated at voltages significantly above the voltage range of the memory array in the second chip (breakdown voltage in the memory array is in the range of one volt), since at the priority date of D1 there were no commercial CCD photodiodes that could be operated at or below the voltage range of the memory. This was not disputed by the appellant, either.

ad (b)

3.5.2 On the other hand, D1/D1a only discloses vias that forward signals from an 8x8 sub-pixel array to the associated A/D converters and to the memory array. This concept of parallel processing of sub-pixel arrays is shown in Figure 5 of D1a. As shown in Figure 31B of D1a, the photosensitive part in D1 during manufacturing is also processed as a separate substrate 57. The same concept is also applied in D4, where the photosensitive part is completely separated from the transistors. This has the advantage that the process technology for the photodiodes does not have to be mixed with the CMOS technology. Both processes require different process steps and materials, so that each substrate can be manufactured more efficiently separately.

3.5.3 The board holds that there are at least four reasons why the skilled person would not route the vias 84'' in Figure 31B of D1 to the surface of chip 57:

(a) The production of vias would require additional process steps in the manufacture of chip 57 that go beyond the production of photodiodes.

(b) In addition, substrate area required for the pixels would be occupied by vias. D1/D1a teaches the concept that only photodiode cells are present in the outer chip 57.

(c) The concept of parallel signal evaluation does not suggest that additional electronics be implemented with which more complex signal evaluation can be performed and which require additional contact vias. Such signal evaluation concepts include, for example, sequential signal readout, i.e. the combination of many pixel signals by sequential readout of the A/D converters. In the present invention, for example, the A/D converters are not read out directly into a memory array as in D1/D1a, but are processed sequentially (see section [0037] of the originally filed application), whereas in D1/D1a the data is stored in the memory array.

(d) Implementing the vias 84'' would require a redesign of the chip electronics and thus require a complete overhaul of the electronic and process technology concept with far-reaching changes in process technology and circuit design.

3.5.4 Consequently, starting from D1/D1a, the skilled person would have no reason to deviate from the signal processing and process technology concept in D1/D1a.

For the above reasons, the teaching of D1/D1a does not suggest implementing the vias 84'' up to the surface of substrate 57.

3.5.5 Furthermore, the board does not see how the teaching of any of the documents D2 to D4 would provide the skilled person with any reason to implement the vias 84'' up to the surface of substrate 57 or to achieve the combination of technical features of claim 1.

3.5.6 D2 discloses two chips, a driver chip and a processing chip, which are designed as stacked chips. In D2, the vias are located in the underlying substrate, which functions as a PCB. The through vias are therefore located in the PCB. The CIS, i.e. the sensing chip, is formed separately in D2 and is not integrated, neither into the first chip, nor into the second chip. Therefore, D2 does not disclose any through vias in the first chip within the meaning of claim 1 of the invention to contact the surface of the second chip.

3.5.7 D3 discloses sensing chips, driver chips and processing chips that are formed separately and adjacent to each other on a substrate. Consequently, D3 does not suggest contacting the second chip through the first chip by means of through vias.

3.5.8 D4 discloses stacked chips. In D4, the processing and driving circuits are housed in one and the same chip. The photodiodes are arranged in the "first chip" without electronics. D4 neither discloses high-voltage transistors in the photosensitive layer, nor different voltages in the first chip and in the second chip. D4 teaches through vias in the "first chip" - not comprising transistors as required by claim 1 of the application - for contacting the second chip. However,

for the reasons stated above, the skilled person would not apply this teaching to the embodiment of Figure 31B of D1a.

3.5.9 The examination division denied inventive step in view of D4 and D3. In paragraph [0056], D4 teaches CMOS electronics, in particular for parallel processing, to be accommodated in the first chip. However, the board is of the opinion that the skilled person would normally start from one of the embodiments in order to solve an objective technical problem (see T 0095/23, catchword) and not from an already complex modification of an embodiment. As in D1, the skilled person would avoid completely redesigning a chip system. If the skilled person were to take up the teaching of D1/D1a, they would attempt to implement parallel processing as taught by D1/D1a in paragraph [0056]. This would possibly lead to a similar structure where there are no through vias in the photosensitive layer any more. This may also lead to a structure where both driver and processing units are still housed together, as already implemented in the embodiment of Figure 9 of D4.

3.5.10 D2 teaches noise avoidance in two stacked chips that do not contain photodiodes, and D3 for chips arranged side by side. Therefore, both documents, D2 and D3 teach operating driver chips and processing chips at different voltages to reduce noise, but in a different context than D4. The skilled person would operate each circuit at as low a voltage as possible, if only to avoid power consumption and overheating. Depending on how processing circuits and driver circuits are distributed in D4, this will be more or less successful. However, none of the documents D1 to D4 gives any precise indication of how the closed circuit block in D4 (the second chip) - comprising both driving

and processing circuitry - is to be divided between the first and second chips.

3.5.11 D1 to D3 each contain, in different contexts, only a partial teaching which the skilled person could take up starting from D4, but which would not lead to all the features of the subject matter of the invention (D1: implementation of parallel processing, but without through vias in the photosensitive layer, D3: noise behaviour in proportion to the breakdown voltages, but for chips arranged next to each other, D2: improved noise immunity for different breakdown voltages in a stacked system not comprising a CIS).

3.5.12 However, none of these documents D1/D1a to D4 provides a precise indication or complete teaching of how the interleaved circuits of driver, power, clock and processing circuitry of the second chip of D4 must be distributed on the first chip and on the second chip, at what voltages these circuitries must be operated and how the wiring between these circuitries must be arranged in light of the partly contradictory teachings of D1/D1a to D4, leading ultimately to the combination of features of the present claim 1, given that the modifications of the embodiment shown in figure 9 of D4 would be too complex.

3.5.13 Consequently, in view of the teachings of D1/D1a to D4, starting either from the embodiment of Figure 31B of D1a or from that of Figure 9 of D4, it is not obvious to arrive at the combination of features (A) to (H).

3.6 Consequently, the subject-matter of claim 1 of the sole request meets the requirements of Articles 52(1) and 56 EPC.

4. Conclusions

4.1.1 The board notes that the description is adapted to the claims and that the relevant prior art is discussed therein.

4.1.2 Since the application meets the requirements of the EPC, the decision under appeal is set aside and the case is remitted to the examining division with order to grant a patent (Articles 97(1) and 111 (1) EPC).

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the examining division with order to grant a patent in the following version:

Description:
pages 1-5, 5a, 5b, filed on 12 December 2019,
pages 6 to 28 as originally filed,

Claims:
no. 1 to 4 filed during oral proceedings before the board on 7 October 2025, titled "Auxiliary Request 2",

Drawings:
Sheets 1/22 to 22/22 as originally filed.

The Registrar: The Chairman:

S. Sánchez Chiquero T. Häusser

Decision electronically authenticated