Internal distribution code:

(A) [-] Publication in OJ
(B) [-] To Chairmen and Members
(C) [-] To Chairmen
(D) [X] No distribution

Datasheet for the decision of 8 December 2025

Case Number: T 1955/23 - 3.4.03

Application Number: 16172382.0

Publication Number: 3101650

IPC: G09G5/36

Language of the proceedings: EN

Title of invention:
METHOD AND APPARATUS FOR PERFORMING INTERLEAVING

Applicant:
Samsung Electronics Co., Ltd.

Headword:

Relevant legal provisions:
EPC Art. 84, 123(2)

Keyword:
Amendments - added subject-matter (no)
Claims - clarity (yes)

Decisions cited:

Europäisches Patentamt
European Patent Office
Office européen des brevets

Beschwerdekammern

Boards of Appeal

Chambres de recours

Boards of Appeal of the
European Patent Office
Richard-Reitzner-Allee 8
85540 Haar
GERMANY
Tel. +49 (0)89 2399-0

Case Number: T 1955/23 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 8 December 2025

Appellant: (Applicant)	Samsung Electronics Co., Ltd. 129, Samsung-ro, Yeongtong-gu, Suwon-si, Gyeonggi-do 16677 (KR)
Representative:	Elkington and Fife LLP Prospect House 8 Pembroke Road Sevenoaks, Kent TN13 1XR (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 19 June 2023 refusing European patent application No. 16172382.0 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	T. Häusser
Members:	A. Böhm-Pélissier
	E. Mille

Summary of Facts and Submissions

I. The appeal is directed against the decision of the examining division refusing European patent application No. 16 172 382 for unallowable amendments (Article 123(2) EPC) and for lack of clarity (Article 84 EPC).

II. The appellant (applicant) **requests** that the decision of the examining division be set aside and the case be remitted to the examining division for further prosecution on the basis of the claims of the main request filed with the letter of 14 October 2025 for the assessment of novelty and inventive step. Alternatively, consideration of the claims of the auxiliary request filed with the grounds of appeal is requested.

III. The wording of **claim 1** according to the **main request** is as follows (feature labelling "(A)", "(B)", ... added by the board):

> *1. (A) A method of performing interleaving, the method comprising:*
> *(B) processing a combination of tiled graphics shader operations and tiled compute shader operations of interdependent render targets; and*
> *(C) interleaving the combination of the tiled graphics shader operations and the tiled compute shader operations, according to a result of the processing,*
> *(D) wherein the processing comprises: analyzing the application programming interface, API, graphics shader calls and API compute shader calls and generating a directed acyclic graph, DAG, of the*

interdependent render targets and interdependent tiles, and using the DAG so as to schedule interleaving of the tiled graphics shader operations and the tiled compute shader operations; and
(E) grouping the API calls so as to build a sequence of interleaved execution of the tiled graphics shader operations and the tiled compute shader operations,
(F) wherein the interleaved and tiled operations are selected such that at least one intermediate data result of a first operation of the sequence is directly read from an on-chip memory by a second operation of the sequence.

IV. The wording of **claims 7 and 8** of the **main request** is as follows (feature labels "(8A)", "(8B)", ... of the features of claim 8 corresponding to features (A), (B), ... of claim 1 added by the board):

7. A computer program comprising computer program codes means adapted to perform all of the steps of any preceding claim when said program is run on a computer.

8. (8A) Apparatus (300) for performing interleaving, the apparatus comprising: a driver (308), configured to:
(8B) process a combination of tiled graphics shader operations and tiled compute shader operations of interdependent render targets; and
(8C) interleave the combination of the tiled graphics shader operations and the tiled compute shader operations, according to a result of the processing,

(8D) wherein the driver (308) comprises: at least one analysis module (312, 314) configured to analyze the application programming interface, API, graphics shader calls and API compute shader calls and generating a directed acyclic graph, DAG, of the interdependent render targets and interdependent tiles, and using the DAG so as to schedule interleaving of the tiled graphics shader operations and the tiled compute shader operations; and

(8E) a scheduling module (330) configured to: group the API calls so as to build a sequence of interleaved execution of the tiled graphics shader operations and the tiled compute shader operations; and

(8F) wherein the interleaved and tiled operations are selected such that at least one intermediate data result of a first operation of the sequence is directly read from an on-chip memory by a second operation of the sequence.

V. The arguments of the appellant as far as they are relevant for this decision can be summarised as follows:

(a) By incorporating the features of dependent claims 2, 8 and 9 as originally filed in claim 1 of the main request the objections under Article 84 and 123(2) EPC are overcome.

(b) This also applies to the corresponding independent claims 7 and 8 of the new main request.

Reasons for the Decision

1. The invention

(a) The present invention addresses inefficiencies in graphics rendering systems, where intermediate rendering steps require frequent access to external memory. This leads to significant memory traffic, which impacts performance and energy efficiency. When generating graphical images, dependencies between render targets (intermediate images) require data to be repeatedly written to and read from external memory.

(b) The solution according to the invention introduces a method to interleave graphics shader and compute shader operations. This interleaving approach processes graphics and compute operations tile-by-tile, allowing intermediate data to remain in the on-chip memory of the GPU (Graphics Processing Unit) instead of being offloaded to external memory. The compute shaders are recompiled to use a tiled access pattern compatible with graphics shaders, enabling efficient memory usage and reduced external memory traffic.

(c) This solution resolves the aforementioned problems as it minimizes the need for external memory access, which reduces bandwidth usage and energy consumption. Additionally, maintaining intermediate computations in the GPU's on-chip memory improves processing speed, leading to better performance in graphics rendering applications (cf. introduction of the description of the present application).

2. **Main request - Article 123(2) EPC**

2.1 The features of claims 1, 2, 8 and 9 as originally filed are incorporated in claim 1 of the main request.

Furthermore, in feature (D) it is specified that the API calls analysed in the analysis module are API graphics shader calls and API compute shader calls. This is supported by page 6, lines 29-30 of the description as originally filed. In the context of claim 8 as originally filed it is evident for the skilled person that the API calls defined in claim 8 correspond to the API graphics shader calls and API compute shader calls in analogy to the graphics shader operations and compute shader operations defined in claim 1 as originally filed.

2.2 The same reasoning applies to the corresponding independent claims 7 and 8, which are additionally based on claims 13 and 14 as originally filed.

2.3 Consequently, the set of claims according to the main request meets the requirements of Article 123(2) EPC.

3. Main request - Article 84 EPC

3.1 The board agrees with the appellant in that the amendments have overcome the clarity objections raised in the impugned decision. The terms of the claims are clear to the skilled person. Features like "(*interdependent*) *render targets*" and "*directed acyclic graph*" (cf. respective *Wikipedia* entries) are part of the knowledge of the person skilled in the present technical field.

3.2 The features of original claim 1 are essential for the invention and are now present in the independent claims 1, 7 and 8 of the main request.

3.3 Consequently, the set of claims of the main request satisfies the requirements of Article 84 EPC.

4. Conclusions

The set of claims of the new main request overcomes the objections under Articles 84 and 123(2) EPC raised in the impugned decision. The decision under appeal does not address the requirements of Articles 52(1), 54(1), (2) and 56 EPC and the appellant has requested remittal to the department of first instance for the assessment of novelty and inventive step. Accordingly, the decision under appeal is to be set aside and the case to be remitted to the examining division for further prosecution pursuant to Article 111(1) EPC. Consideration of the auxiliary request is not necessary.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the examining division for further prosecution.

The Registrar: The Chairman:

S. Sánchez Chiquero T. Häusser

Decision electronically authenticated