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Bezeichnung der Erfindung:
Title of invention: Semiconductor memory
Titre de l'invention :

Klassifikation / Classification / Classement : G11C11/40

ENTSCHEIDUNG / DECISION

vom / of / du 28 May 1985

Anmelder / Applicant / Demandeur : Fujitsu Ltd.

Patentinhaber / Proprietor of the patent / Titulaire du brevet : ////////////////

Einsprechender / Opponent / Opposant : ////////////////

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Art.52(1),56

"Inventive step"

Leitsatz / Headnote / Sommaire

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Case Number: T 145 / 82

DECISION

of the Technical Board of Appeal 3.5.1

of 28 May 1985

Appellant: Fujitsu Limited
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Decision under appeal: Decision of Examining Division 067 of the European Patent Office dated 07-05-1982 refusing European patent application No 79302334.2 pursuant to Article 97(1) EPC

Composition of the Board:

Chairman: G. Korsakoff
Member: J. van Voorthuizen
Member: F. Benussi

Summary of Facts and Submissions

I. European Patent Application No. 79 302 334.2 filed on 25.10.79 (Publication No. 0 011 405) claiming a priority of 30.10.78 (JP), was refused by a decision of the Examining Division 067 of the EPO of 07.05.82. That decision was based on Claim 1 filed 26.01.82 and Claims 2-5 as originally filed.

II. The reason given for the refusal was that the subject-matter of the claims lacked inventive step with regard to US-A-3 747 078 and IEEE, Journal of Solid State Circuits, Vol.SC-6, No. 5, October 1971, pages 283-288.

III. The Applicant lodged an appeal against this decision on 01.07.82. The Statement of Grounds was filed on 08.09.82. The appeal fee was paid on 05.07.82. The Statement of Grounds was accompanied by amended Claims 1-6.

IV. In a communication of 18.10.83 the Rapporteur of the Board of Appeal set out a number of objections to the then valid claims.

V. In his Statement of Grounds and in the reply of 24.01.84 to the aforesaid communication the Appellant essentially argued as follows :

The article in IEEE Journal of Solid State Circuits merely discloses the use of bipolar transistors in memory cells. US-A-3 747 078 is not concerned with the problem of an uneven distribution of holding currents to memory cells connected along a common word line, as is the present application, but with the problem of obtaining equal output signals from memory cells connected along a particular bit-line when the cells are sensed. The solution proposed in this US patent is variation of the impedances of transistors

coupling the storage cells to the bit-lines and this does not suggest the possibility of varying an element of the storage cell itself. Finally, this document is concerned only with FET devices and not with bipolar transistors as used in the memory according to the present application. The US patent therefore does not lead a person skilled in the art to the claimed invention.

Moreover an article in IEEE Transactions on Electron Devices, June 1979, pages 886-892, published after the priority date of the application but before its publication date, shows that the author of that article considered that the problem still existed and failed to find the solution put forward by the present invention.

VI. The Appellant maintains his request that a European patent be granted on the basis of Claims 1-6 filed on 08.09.82.

These claims read as follows :

1. A semiconductor memory having a plurality of memory cells (CEL) which are formed by bipolar transistors (Q_1, Q_2, Figure 5; Q_3 to Q_6, Figure 7) and which are connected to different points along common word lines (W+, W-) and a constant current source which is connected to the end of a word line (W-) and which passes hold current to or from the memory cells, characterized in that the areas of the emitter regions (E_1, E_m) of memory cell transistors passing the hold current differ with the position of the memory cell along the word line, whereby the hold currents of the different memory cells are substantially uniform regardless of the positions of the memory cells along the word lines and the information stored in the memory cells is prevented from inverting.

2. A semiconductor memory according to Claim 1, characterized in that the areas of the emitter regions differ from memory cell to memory cell along its word lines.

3. A semiconductor memory according to Claim 1, characterized in that the areas of the emitter regions differ from one group of memory cells to the next group of memory cells along the word lines.

4. A semiconductor memory according to Claim 1, characterized in that the memory cell includes first and second resistors (r_1, r_2) which are connected to a first of the word lines (W+), the collectors of the first and second of the pair of transistors (Q_1, Q_2) being respectively connected to the other ends of the first and second resistors, the emitters of the first and second transistors being commonly connected to the second word line (W-), the base of the first transistor being connected to the collector of the second transistor, and the base of the second transistor being connected to the collector of the first transistor.

5. A semiconductor memory according to Claim 1, characterized in that the memory cells are of the integrated injection logic type and the said pair of transistors (Q_3, Q_4, Figure 7) are of a first conduction type and have a common emitter forming an injector connected to a first of the word lines, each memory cell further including third and fourth transistors (Q_5, Q_6) of a second conduction type each of which has a collector (N_1 N_2) connected to a respective collector (P_3 P_2) of the first and second transistors (Q_3, Q_4), the base of the third transistor (Q_5) being connected to the collector of the fourth transistor (Q_6), the base of the fourth transistor being connected to the collecotr of the third transistor,

and the first and second transistors having bases which are connected to the emitter of the third and fourth transistors and to a second of the word lines.

6. A semiconductor memory in accordance with any one of the preceding claims, in which the areas of the emitter regions are varied with the position of the memory cell along the word line by extending the emitter in a direction perpendicular to the direction of current flow through the transistor.

Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is, therefore, admissible.

2. The problem which the present application sets out to solve is the following : in a memory formed by a plurality of memory cells each constituted by a bistable circuit of bipolar transistors, the holding currents provided to the cells by word lines differ from cell to cell owing to the resistance of the word lines, the cells all having the same impedance. Memories of the kind referred to are well known, as is evidenced by the documents cited in the search report and as admitted by the Appellant. Also well known is the fact that the interconnecting lines in such memories (word or bit lines) may have an undesirable resistance.

3. The person skilled in the art will readily recognize that the differences in holding current are caused by the resistance of the word line. In the past, a certain non-uniformity of these currents has been accepted (at the cost of increased power dissipation), so long as the minimum holding

current to any cell was high enough to prevent the cell from being inverted by noise. (Cf. page 1 of the description, lines 20-27).

4. More recently, however, power considerations have been carrying greater weight in the development of memories having ever-increasing bit densities. The person skilled in the art faced with the above problem will therefore, as a matter of course, look for solutions in which power is saved i.e. in which all the holding currents have the minimum value acceptable, taking into account noise considerations, so that all the cells operate under essentially identical conditions.

5. US-A-3 747 078 concerns the problem that due to resistance in the bit-lines (sense lines) of a memory, equal signals sensed at different cells connected to the same bit-line produce signals at the sense amplifier end of such line which are smaller the further a cell is remote from that end. Although in the preferred embodiment described in this patent FET devices are used it appears from the context (e.g. Claim 1) that also other transistor types could be used. The solution proposed consists in a gradation in impedance of the coupling devices along the sense lines so that variation in load impedances for the cell due to the sense line resistance is compensated for.

6. The Board is of the opinion that a person skilled in the art faced with a problem in a memory caused by the resistance of the word lines will appreciate that the US patent deals with a related problem. Although the Applicant is right in pointing out that the problem the US patent is concerned with is not that of an even sharing of currents applied to cells connected to a same word line, both problems have in

common that they are basically caused by the fact that a number of devices having equal (input or output) impedances are connected along a resistive line.

7. The solution to the specific problem dealt with in the US patent is of course not directly applicable to the problem dealt with in the present application. Nevertheless this citation teaches that by suitably adapting the impedances of individual cells connected to the same line, essentially identical operating conditions for all the cells can be established and, further, that not all cells need be of identical construction as has customarily been the case.

8. It will be evident to the person skilled in the art that, in the memory systems to which the present application refers, it is the holding current of the bistable circuit that has to be influenced and that this can only be attained by changes in the bistable circuit, irrespective of the presence or absence of coupling devices to the connecting lines.

9. As is apparent from the generally known formula (4) on page 7 of the description, the emitter current value of a p-n junction at a given voltage is determined by the emitter area. Such a junction can be considered as a voltage dependent non-linear resistance. Furthermore, it is well known that the holding current for a bistable memory cell can be chosen within rather wide limits consistent with power and noise considerations.

10. In view of the foregoing, the Board has come to the conclusion that a person skilled in the art would logically arrive at the solution described in Claim 1 on the basis of knowledge and skill normally to be expected of him. Claim 1 is therefore unallowable, as not involving an inventive step within the meaning of Article 56 EPC.

11. With regard to paragraph 4 of the Appellant's letter of 24.01.84, the Board observes that it is not unusual in a field undergoing development that, at about the same time, different solutions to a same problem are independently proposed. However, no conclusions can be drawn from this fact as to the inventive step present in either of these solutions.

12. The objections against the dependent claims formulated in the communication by the Rapporteur of 18.10.83 have not been refuted by the Appellant. Consequently, these objections are maintained and these claims also are unallowable.

Order

For these reasons it is decided that :

The appeal is dismissed.

The Registrar — The Chairman

B A Norman — G Korsakoff