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Titre de l'invention :

Klassifikation / Classification / Classement : G 06 F3/04

ENTSCHEIDUNG / DECISION

vom / of / du 9 December 1985

Anmelder / Applicant / Demandeur : Fanuc Ltd.

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Article 56
"Inventive step"

Leitsatz / Headnote / Sommaire

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Case Number: T 54 / 83

DECISION

of the Technical Board of Appeal 3.5.1

of 9 December 1985

Appellant: Fanuc Ltd.
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Oshino-mura, Minamitsuru-gun
JP - Yamanashi Prefecture

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Decision under appeal: Decision of Examining Division 065 of the European Patent Office dated 18.10.1982 refusing European patent application No 80 300 135.3 pursuant to Article 97(1) EPC

Composition of the Board:

Chairman: G. Korsakoff

Member: J. Van Voorthuizen

Member: P. Ford

I. Summary of Facts and Submissions

I. European patent application No. 80 300 135.3 filed on behalf of the Appellants on 15.01.80 (publication No. 0 015 054) claiming a priority of 17.01.79 (JP) was refused by a decision of the Examining Division 065 of the EPO dated 18.10.82. That decision was based on Claims 1-7 as originally filed.

II. The reason given for the refusal was that the subject-matter of Claim 1 was not novel over US-A-4 034 346. If the claims were limited in a certain way based on arguments provided in the Appellants' letter of 17.06.82, such claims would lack inventive step having regard to Giebler, Elektrie, 1978, pages 636-639, GB-A-1 533 576 and US-A-4 034 346.

III. The Appellants lodged an appeal against this decision on 13.12.82 and paid the appeal fee on 15.12.82. The Statement of Grounds was filed on 22.02.83, accompanied by amended Claims 1-7.

IV. In a communication of 05.03.85 the Rapporteur of the Board of Appeal formulated objections against the then effective claims.

V. On 09.12.85 oral proceedings were held at the Appellants' request. In the course of these proceedings, the Board drew the Appellants' attention to several passages of the book "Computer Engineering" by Bell, Mudge, McNamara (September 1978) which concern the use of buses in parallel.

VI. In the Statement of Grounds, in the reply to the Rapporteur's communication, in the course of the oral proceedings and in a letter filed 06.02.86 the Appellants argued essentially as follows:

From the documents cited by the Examining Division and by the Board of Appeal taken singly or in combination, the subject-matter of claim 1 could not be derived in an obvious manner, as none of them refers to delay problems caused by limited FAN-OUT capabilities or shows the use of two bidirectional buses in parallel connected via driver/receiver circuits to a central processing unit (CPU). The article by Giebler teaches the use of one universal I/O bus, to which all peripheral circuits are connected except two (ZVZ and ABD) which are of a particular character. Even if the channel to which these are connected were regarded as a bus, it could and would probably be driven directly by the CPU, without driver/receiver circuits. US-A-4 034 346 shows a data processing unit star connected by external data links (which on the normal meaning of the term do not constitute buses) to a number of remote working stations, each comprising several items of data emitting and receiving apparatus. Separate lines are used for transmission in opposite directions and the bits are serially transmitted. There is no disclosure that data are transferred to or from the CPU (although this might form part of the complete data processing unit) or that the transmitters/receivers are controlled by such a CPU. The present application concerns internal bidirectional buses using parallel transmission of bits between a CPU and peripheral circuits all within the same data processor unit.

VII. The Appellants requested the grant of a European patent on the basis of the following items:

Main request : Claims 1-7 as filed on 22.02.83
Auxiliary request 1: Claim 3 as filed on 22.02.83
Auxiliary request 2: Claim 7 as filed on 22.02.83

These claims read as follows :

1. A bus connection system for a data processor unit in which transmission and reception of data between a central processing unit and each of a plurality of peripheral circuits is effected via a bidirectional bus which is connected to the central processing unit by a driver and a receiver,
characterised in that there are provided :
a first bidirectional bus connected to each of a first plurality of peripheral circuits,
a first driver and a first receiver for connecting the central processing unit to the first bidirectional bus under control of the central processing unit,
a second bidirectional bus connected to each of a second plurality of peripheral circuits, and
a second driver and a second receiver for connecting the central processing unit to the second bidirectional bus under control of the central processing unit.

2. A bus connection system according to Claim 1, wherein the central processing unit, the first and second drivers and the first and second receivers are provided on one printed circuit board.

3. A bus connection system according to Claim 1, for a data processor unit having first and second interconnected central processing units, wherein the first and second drivers and first and second receivers are for connecting the first central processing unit to the first and second bidirectional buses, and wherein third and fourth drivers and third and fourth receivers are provided for connecting the second central processing

unit to the first and second bidirectional buses, the third driver and third receiver being coupled to the first bidirectional bus and the fourth driver and fourth receiver being coupled to the second bidirectional bus.

4 A bus connection system according to any preceding claim, wherein at least one of the peripheral circuits is an input/output control circuit.

5. A bus connection system according to any preceding claim, wherein at least one of the peripheral circuits is an external memory.

6. A bus connection system according to Claim 5, wherein the peripheral circuits comprise a plurality of external memories each of which is a low capacity memory loaded on a printed circuit board.

7. A bus connection system according to Claim 1, comprising a back panel for mounting a plurality of printed circuit boards respectively carrying the central processing unit and peripheral circuits, the back panel having a plurality of buses formed thereon with connectors for receiving the printed circuit boards, wherein the printed circuit board carrying the central processing unit, when mounted on the back panel, is connected for the passage of data along each of the buses, and wherein each printed circuit board carrying a peripheral circuit, when mounted on the back panel, is connected for the passage of data along a selected bus only.

II. Reasons for the Decision

1. The appeal complies with Articles 106 and 108 and Rule 64 EPC and is, therefore, admissible.

2. The present application is concerned with the problem that the number of peripheral circuits which can be connected to a bus is limited by the fan-out capacity of the bus driver and by the delay caused by an increase in the bus length. Is it proposed to alleviate this problem by the provision of two buses, both connected to the central processing unit (CPU) via respective drivers and receivers.

3. A bus connection system as referred to in the preamble of Claim 1 is of conventional type as is also admitted in the description of the application, page 2, first line and lines 31-33. An example of this is shown in the article by Giebler in "Elektrie", Ed. 32, 1978, pages 636-639. From the book "Computer Engineering" by Bell, Mudge, McNamara (Digital Press, September 1978) page 276, it is known that increasing the number of connections to the bus (FAN-OUT) or increasing its length leads to an increase of the propagation delay. It is suggested to remedy this effect by inserting a bus repeater circuit but the Appellants point out in their letter of 06.02.86 (page 2) that it is not clear that such a repeater would serve to reduce the delay of waveform caused by the increases in the bus length and FAN-OUT.

4. Under these circumstances, it appears to the Board that the person skilled in the art confronted with the problem that the desired number of connections to a bus would exceed its capacity, is left only with the option to distribute the load over several buses connected in parallel. This solution seems the more obvious since it was already known to provide buses in parallel in data processor systems. Fig. 8 on page 279 of "Computer Engineering" shows a configuration with two "Mass buses" in parallel which are connected to the CPU via two controllers and a Unibus. Fig. 10 on p. 424 of the same book shows the use of four "Mass buses" in parallel which are connected to the CPU via

a cache memory. No explicit explanation is given for the use of several buses in parallel but it is quite obvious that this permits the data processor to be connected to a larger number of peripheral equipments then would be possible if only one bus were used. Even if it is accepted that the Mass buses serve to connect external peripheral equipment to a data processor unit, this is considered as irrelevant as the problems of connecting a multiplicity of peripheral equipment to a same data processor unit or to a same central processing unit are fundamentally the same.

5. The Appellants' representative in his letter of 06.02.86 rightly points out that the configurations shown as a whole are different from the configuration according to the present application and that in particular the "Mass buses" are not in "direct" communication with the CPU. Nevertheless, it still remains the CPU which controls the passing of data between itself and the peripheral circuits.

6. As far as US-A-4 034 346 is concerned, the Board notwithstanding the Appellants' arguments, is of the opinion that the data links between the data processor and the working stations have to be considered as being at least very similar to buses, if only for the fact that several items of peripheral equipment are connected to the same link, are individually addressable and share the same data transmission lines. Moreover, the data processing unit must necessarily comprise a CPU controlling the flow of data to and from the items in the working stations. The US patent must therefore be considered also as disclosing the use of buses in parallel for connecting a central processor to peripheral equipments.

7. As it is conventional to use a driver and a receiver controlled by the CPU with a single bidirectional bus, it must be obvious to use a driver and a receiver controlled by the CPU with each bus whenever more than one bus is used. There is nothing in the present application or in any material presented on behalf of the Appellants that indicates that any particular difficulties had to be overcome or that any unexpected benefits are obtained from the alleged invention.

8. For all these reasons, the Board finds that Claim 1 does not involve inventive step.

9. In accordance with the Appellants' auxiliary request, the Board has examined the allowability of Claims 3 and 7.

10. Claim 3 relates to the application of the basic idea which is the subject of Claim 1 in the case of two cooperating CPU's. Data processor systems in which several CPU's cooperate are generally known. More particularly, a configuration in which two coupled CPU's are used is shown in Fig. 8 on page 248 of "Computer Engineering". Each processor is connected to one bus controlled by its respective processor as the Appellants correctly observe, and both buses are coupled to a further bus to which peripheral circuits are connected which can be shared by both CPU's. It is clear that the problem of bus overload may also arise if two CPU's are used in a data processor. Once the idea of using two buses in parallel to accommodate more peripheral circuits has to be implemented in the case of two CPU's the Board considers that the person skilled in the art would naturally think of applying the conventional drivers and receivers controlled by the CPU. The embodiment of Claim 3 should apparently provide for access by both CPU's to all peripheral circuits. Taking this into account, the person skilled in the art must inevitably arrive at the

configuration of drivers and receivers which is stated in the characterising part of Claim 3. The Board, therefore, is unable to see inventive step in the subject-matter of Claim 3 any more than in that of Claim 1.

11. Concerning Claim 7, is has to be observed that assembling a CPU and its peripheral circuits by means of a number of printed circuit boards connected to a mother board which carries a bus is common practice; see for example, the article by Giebler and GB-1 533 576. It is self evident that this manner of assembling can be applied in the case where two buses are present and in the Board's opinion no inventive matter is conferred by the addition of features relating to this manner of assembling the components of the data processor system to the subject-matter of Claim 1.

Order

For these reasons it is decided that :

The appeal is dismissed.

The Registrar — The Chairman

B A Norman — G Korsakoff