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Bezeichnung der Erfindung: A decoder circuit for a semiconductor memory device
Title of invention:
Titre de l'invention :

Klassifikation / Classification / Classement : H03K 13/25

ENTSCHEIDUNG / DECISION

vom / of / du 22 February 1988

Anmelder / Applicant / Demandeur : Fujitsu Limited

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Article 56

Kennwort / Keyword / Mot clé : "Inventive step"

Leitsatz / Headnote / Sommaire

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Case Number : T 75/84

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 22 February 1988

Appellant : FUJITSU LIMITED
1015, Kamikodanaka Nakahara-ku
Kawasaki-shi Kanagawa 211
JP

Representative : Rackham, Stephen Neil
GILL JENNINGS & EVERY
53-64 Chancery Lane
London WC2A 1HN
GB

Decision under appeal : Decision of Examining Division 068 of the European Patent Office dated 24 October 1983 refusing European patent application No. 80 301 175.8 pursuant to Article 97(1) EPC

Composition of the Board :

Chairman : P.K.J. van den Berg
Members : W.B. Oettinger
F. Benussi

Summary of Facts and Submissions

I. European Patent application number 80 301 175.8 filed on 11 April 1980 claiming a priority of 26 April 1979 and published under number 18 739 was refused by a decision of the Examining Division 2.2.01.068, the draft original of which had been signed by the members of the competent division on 5 August 1983.

According to the file, a first despatch dated 14 October 1983 of a decision of the same content did not bear the correct names of all three members of the competent Examining Division; the name of the second member was replaced by the name of an examiner not involved.

A second despatch of that decision, dated 24 October 1983 and complemented - according to the file - by the (handwritten) sentence "This communication cancels and replaces the communicated dated 14.10.83", did bear the correct names of all three members involved.

II. The reason given in the decision for the refusal was that the subject-matter of independent Claim 2 filed on 12 July 1983 - disregarding a feature which had been inserted by an amendment contravening Art. 123(2) EPC - lacked an inventive step having regard to the prior art.

The one alternative form of that subject-matter, implemented in the embodiment described with reference to Figure 3, was found obvious with regard to US-A-3 914 620 alone and the other, implemented in the embodiment of Figure 4, obvious with regard to the same document in combination with US-A-3 624 620.

Referring to the objection made in an official communication dated 23 March 1982, the Examining Division drew the same conclusion for the dependent Claims 3 and 4 filed on 12 July 1983.

In the decision under appeal, Claim 1 filed on 30 May 1983 was also rejected because it was found only to recite the features of original Claims 1,2 and 4 which were held, according to the earlier communication, not to involve an inventive step. Only at first sight this claim appeared to follow a suggestion, made at a previous interview, to draft a claim based on the arrangement shown in Figure 6. In that interview, the Primary Examiner expressed his provisional opinion that such a claim would appear acceptable.

III. On 21 December 1983, the Applicant lodged an appeal against the decision to refuse, referring to that decision as "dated 24 October 1983", and paid the appeal fee on 24 December 1983.

A statement of grounds of appeal was filed on 1 March 1984 together with new Claims 1 to 4 so amended as to overcome any Art. 123(2) EPC objection.

In the grounds, the Appellant submitted that the lack of inventive step objection was unjustified.

IV. In a communication dated 26 November 1985, the Board expressed reservations as to an inventive step of the embodiments of the claimed invention which are described with reference to Figure 3 and 4 (Claim 1).

In support of these reservations, the Board produced, in addition to the above cited prior US specifications, the following further prior document: IBM Technical Disclosure Bulletin, Volume 18, No. 11, April 1976, pages 3597/3598.

It concluded that it is obvious to modify a decoder circuit as known, in effect, from the cited US-A-3 914 620, in a way as suggested by the IBM disclosure.

No such conclusion was however drawn for the embodiment described with reference to Figure 6 (then Claim 4).

V. In a response filed on 1 August 1986, the Appellant disagreed with the Board's provisional finding as far as the Figure 3 and 4 embodiments are concerned and submitted that the claimed invention is contrary to the development of the art as outlined in the US citation, and that it is therefore not obvious to combine any "background" prior art not recommended in the US citation with the teaching of the IBM citation.

Further he relied on specific advantages achieved by the claimed invention in respect of the required number of constant current sources, i.e. power consumption, and in respect of speed of operation.

VI. In a second communication dated 30 April 1987, the Board pointed out some inconsistencies between the prior art as acknowledged in the application with reference to Figure 1A and 2 and the prior art as disclosed in the "background" and "invention" parts of the US citation and, further, a lack of clarity as to the function of the earlier prior art.

Furthermore, the Appellant's arguments based on the achievement of specific advantages were found unconvincing.

It therefore extended its lack of inventive step reservations even to the Figure 6 embodiment.

VII. In a response filed on 7 January 1988 the Appellant maintained his position but gave some explanation in respect of the prior art and the claimed invention.

VIII. He requests that the decision under appeal be overturned and a patent be granted on the basis of the amended application documents.

According to the file these include:

description pages 1 and 4 filed on 7 January 1988,
pages 2 and 5 to 7 filed on 1 August 1986,
page 2a filed on 1 March 1984,
page 3 as published;

Claims 1, 2 and "4" part 1 filed on 1 August 1986, part 2 filed on 1 March 1984, renumbered "3" on 21 August 1986;

drawings sheet 1 to 6 as published.

Alternatively, if Claims 1 and 2 are found unallowable, the Appellant requests a decision based on Claim 3 as the only claim and giving the Appellant an opportunity to make further amendments as found necessary.

IX. The independent claims, directed to the embodiments of Figure 3 and 4 and to the embodiment of Figure 6, respectively, read as follows:

"1. A decoder circuit for a semiconductor memory device comprising a sequence of address signal input terminals (A_0, A_1, ... A_n), a number of address buffers (21, 22, ... 2n), each of which includes a gate circuit for producing an

address signal and an inverted address signal, a constant current source (S_1) connected to the gate circuit, and transistors (Q_E) connected in an emitter follower configuration to form each output of the gate circuit, a number of pairs (d_0, $\bar{d}_0$; d_1, $\bar{d}_1$; ... d_n, $\bar{d}_n$) of decoder lines (3) connected to the transistors (Q_E) with one of each pair (d_0, d_1, ... d_n) of decoder lines being connected to the emitter follower connection transistor (Q_E) producing the address signal and the other of each pair ($\bar{d}_0$, $\bar{d}_1$, ... $\bar{d}_n$) of decoder lines (3) being connected to the emitter follower connection transistor (Q_E) producing the inverted address signal, each pair (d_0, $\bar{d}_o$; d_1, $\bar{d}_1$; ... d_n, $\bar{d}_n$) of decoder lines (3) being connected between its emitter follower connection transistor (Q_E) and an additional constant current source (S_2'), each decoder line (d_0, $\bar{d}_0$, d_1, $\bar{d}_1$, ... d_n, $\bar{d}_n$) including a series connected switching transistor (Q_a, Q_b) having its base connected to the other decoder line (d_o, d_1, ... d_n or $\bar{d}_0$, $\bar{d}_1$, ... $\bar{d}_n$) of that pair so that a major part of the current from each additional constant current source (S_2') passes through only one decoder line (d_0, d_1, ... d_n or $\bar{d}_0$, $\bar{d}_1$, ... $\bar{d}_n$) of each pair of decoder lines (3) at any instant, a sequence of word lines (W_0, W_1, ... W_n), and a number of word drivers (41, 42, ... 4n) each having a matrix of diodes (D_1, D_2, ... D_n) or a multi-emitter transistor (Q_m), a resistor circuit (R_0) connected to a power source, and a transistor (Q_w) connected to one of the word lines (W_0, W_1, ... W_n), one end of each of the diodes (D_1, D_2, ... D_n) or each emitter of the multi-emitter transistor (Q_m) being connected to one of the decoder lines (d_0, $\bar{d}_0$, d_1, $\bar{d}_1$, ... d_n, $\bar{d}_n$) and the other end of each diode (D_1, D_2, ... D_n) or the collector of the multi-emitter transistor (Q_m) being connected to a junction of the resistor circuit and the base of said transistor (Q_w) connected to one of the word lines (W_0, W_1, ... W_n)

3. A decoder circuit for a semiconductor memory device comprising a sequence of address signal input terminals (A_0, A_1, ... A_n), a number of address buffers (21, 22, ... 2n), each of which includes a gate circuit for producing an address signal and an inverted address signal, a constant current source (S_1) connected to the gate circuit, and transistors (Q_E) connected in an emitter follower configuration to form each output of the gate circuit, a number of pairs (d_0, $\bar{d}_0$; d_1, $\bar{d}_1$; ... d_n, $\bar{d}_n$) of decoder lines (3) connected to the transistors (Q_E) with one of each pair (d_0, d_1, ... d_n) of decoder lines being connected to the emitter follower connection transistor (Q_E) producing the address signal and the other of each pair ($\bar{d}_0$, $\bar{d}_1$, ... $\bar{d}_n$) of decoder lines (3) being connected to the emitter follower connection transistor (Q_E) producing the inverted address signal, each pair (d_0, $\bar{d}_0$; d_1, $\bar{d}_1$; d_n, $\bar{d}_n$) of decoder lines (3) being connected between its emitter follower connection transistor (Q_E) and an additional constant current source (S_2'), each decoder line (d_0, $\bar{d}_o$, d_1, $\bar{d}_1$, ... d_n, $\bar{d}_n$) including a series connected switching transistor (Q_a, Q_b) and resistor (R_a, R_b), the bases of the emitter follower configuration transistors (Q_E) being connected to the bases of the switching transistors (Q_a, Q_b) by level changing circuits including level shifting diodes (D_a, D_b) and other current sources (S_{23}'), to obtain a quick start to the charging of the decoder lines (d_0, $\bar{d}_0$, d_1, $\bar{d}_1$, ... d_n, $\bar{d}_n$), and to ensure that a major part of the current from each additional constant current source (S_2') passes through only one decoder line (d_0, d_1, ... d_n or $\bar{d}_0$, $\bar{d}_1$, ... $\bar{d}_n$) of each pair at any instant, a sequence of word lines (W_o, W_1, ... W_n), and a number of word drivers (41, 42, ... 4n) each having a matrix of diodes (D_1, D_2, ... D_n) or a multi-emitter transistor (Q_m), a resistor circuit (R_0) connected to a power source, and a

transistor (Q_W) connected to one of the word lines (W_0, W_1, ... W_n), one end of each of the diodes (D_1, D_2, ... D_n) or each emitter of the multi-emitter transistor (Q_m) being connected to one of the decoder lines (d_0, $\bar{d}_0$, d_1, $\bar{d}_1$, ... d_n, $\bar{d}_n$) and the other end of each diode (D_1, D_2, ... D_n) or the collector of the multi-emitter transistor (Q_m) being connected to a junction of the resistor circuit and the base of said transistor (Q_w) connected to one of the word lines (W_0, W_1, ... W_n)."

Dependent Claim 2 concerns a particular embodiment of the circuit of Claim 1 having the feature described with reference to Figure 5.

Reasons for the Decision

1. The appeal complies with Art. 106, 107, the first two sentences of Art. 108, and Rule 64 EPC.

In the communication, dated 14 October 1983, of the decision taken by the competent Examining Division on 5 August 1983, a wrong name for one of the members involved in the decision was mentioned.

When the error was noticed, a second despatch with the correct names was sent to the Appellant on 24 October 1983 which replaced the first one, and this the more so because of the (handwritten) sentence on this second despatch as mentioned under item I of this decision. The second despatch is therefore the only act producing effects in respect of the time limit within which the Appellant should have filed the statement of grounds.

With regard to these circumstances it appears clear that the statement of grounds of appeal was filed within the time limit prescribed by Art. 108, third sentence, EPC.

The appeal is therefore admissible.

2. The amendments made to the application documents are admissible under Art. 123(2) EPC.

2.1 Claim 1 is based on original Claim 2, and all additional features are disclosed in Figures 3 and 4 and the relevant part of the description.

Dependant Claim 2 adds the feature of the original Claim 3 also shown in Figure 5.

Claim 3 is based on the original Claim 4 in its dependence on foregoing original Claims 1-3 and all additional features are disclosed in Figure 6 and its description.

2.2 The amendments made to the description so far do also not introduce new matter; mostly they concern the correction of errors (e.g. on page 1 and page 4) which are obvious in the circumstances.

3. While the subject-matter of Claim 1 is clearly new, in the opinion of the Board, it must be considered as not involving an inventive step.

This finding is, in essence, based on the consideration that, although the subject-matter claimed does not follow the development of the relevant art as outlined in the cited US-A-3 914 620, it departs from this development only in a way which is obvious with regard to the general knowledge of the skilled person and to the IBM citation.

3.1 The prior art which is relevant to the claimed invention may be described as follows:

(a) The "background" part of the US citation (col. 1 lines 5 to 36) discloses an earlier prior art of decoder circuit comprising:

- address buffers consisting of an emitter coupled logic inverter, including load resistors, and a pair of emitter followers,

- an OR'ing circuit, multiple emitter transistors being used as emitter followers and current sources being a pre-requisite for the functioning of these emitter followers,

- word drivers consisting of an emitter coupled logic inverter, including - of course - collector resistors, and a NOR gate, the latter having multiple inputs.

Figure 1A of the application allegedly (page 3, lines 24 and 25) also shows an earlier prior art. Its address buffers and word drivers are similar to those in the US "background" but, instead of multiple emitters of the emitter followers, an OR'ing circuit and multiple inputs to the NOR gates, pairs of decoder lines are so connected between the address buffers and the word drivers that the same decoding function is achieved.

It is therefore considered that Figure 1A represents an (undocumented in the sense of Art. 54(2) EPC) equivalent to the US "background".

(b) The "invention" part of the US citation discloses a prior art of decoder circuit.

In this circuit,

- the address buffers consist of an emitter follower and an emitter coupled logic inverter, not having load resistors,

- there are no constant current sources connected to the paired decoder lines,

- the word drivers consist of a diode logic, including a load resistor, and an emitter follower.

Figure 2 of the application allegedly shows a similar decoder circuit. Its address buffer does not have the emitter follower; its emitter coupled logic circuit does however include load resistors, in other respects there being no difference.

Figure 2 may therefore be regarded as representing an (undocumented in the sense of Art.54(2) EPC) equivalent to the US "invention".

(c) According to the US citation, the "later" prior art has the advantage over the "background" art of an extremely fast speed of operation (Col. 3, lines 37 to 38) and a far less power dissipation (lines 49 to 50). The fast speed is mainly achieved by the omission of the load resistors and of the emitter followers (Col. 3, lines 39 to 49) and the low power consumption by the modified interconnecting scheme (lines 50 to 58) requiring less current sources.

(d) The IBM citation discloses an address buffer inverter which comprises an inverter (T8, T7) performing the same function as an emitter coupled logic inverter,

and transistors (T3, T4) performing the same function as, or even being, emitter followers.

This address buffer inverter is relevant in the present case because it has a pair of switching transistors (T10, T11) coupling the output lines to a current source in a mode complementary to the operation of the emitter followers.

The fact that it has, in addition, a number of gates (T9, T1, T2, T5, T6) in the inverter and another gating circuit (IG) in the circuit of the switching transistors, which do not seem to be required in such a decoder circuit, does not render this prior art less relevant.

It is further relevant for the reason that it is clearly implicit in this document that its address buffer inverter can be part of a decoder circuit having further parts such as those disclosed in the US citation.

3.2 In this prior art situation the question to be answered is whether it is obvious, starting from the "background" art, to maintain, or, starting from the "later" prior art, to re-introduce, the emitter followers in the address buffer and to add to these, as is known from the IBM citation, the current switching transistors.

In the opinion of the Board this question must be answered in the affirmative for the following reasons:

3.3 While it is true that from the development of the art as disclosed in the US citation alone it would not follow that there is a reason for the skilled person to disregard the "later" prior art and modify the "background art" instead,

there is such a reason when the other prior art, read with the general knowledge of the skilled person, is taken into account.

This reason is seen in the fact that it will be obvious to the skilled person that the omission of emitter followers following the emitter coupled logic inverter is not in any case the optimum solution but, under certain circumstances, an advantage can be expected from complementing the emitter followers with switching transistors as disclosed in the IBM citation.

That this expectation can be justified, follows also from the Appellant's explanations. More particularly:

3.4 According to the IBM citation, switching transistors ensure that, whenever one of outputs (SAR, $\overline{SAR}$) is raised by one of the emitter followers (T3, T4) to the voltage level DCS, the respective other output line is clamped to ground potential (page 3598).

According to the Appellant, in the claimed invention the switching transistors ensure that whenever one of the decoder lines is pulled up, by one of the emitter followers (QE) to a high voltage, the respective other decoder line is pulled down to the lower constant current source potential.

These functions are clearly identical.

3.5 According to the US citation (Col. 3, line 39), (a) the speed of operation of the "later" prior art is determined by the delay of one emitter coupled logic inverter, and (b) from the expressed fact (column 3, lines 40-41) that the diode logic functions as the load circuitry for the emitter coupled logic inverter, it follows directly that the time

constant given by one decoder line capacity and the diode logic resistance produces an additional delay degrading the speed of operation.

Insofar as the communication dated 30 April 1987 relied on the "extremely fast" speed of operation allegedly achieved by the US decoder circuit it should be mentioned that this opinion was not final and had to be reconsidered in the light of the Appellant's submission based on Column 3, lines 40 to 42 of the US citation.

From the IBM citation it follows that (a) the speed of operation is determined also by the delay of one logic inverter and that (b) the delay produced by one output driver and its complementary switching transistor would degrade the speed of operation additionally. But apparently, there is no resistor which would, together with the capacity of the output line, which may be a decoder line, introduce a further time constant.

Thus it must be regarded as obvious for the skilled person that the additional delay introduced by the output drivers (IBM) may or may not be larger than that introduced by the diode logic resistor in conjunction with the decoder line capacity (US), depending, for instance, upon the properties of the decoder lines. It will therefore depend on the circumstances whether the skilled person can expect an advantage in this respect from the IBM disclosure. This fact will be reason enough for him not to disregard this possible alternative to the "later" US prior art from the beginning, but to consider seriously whether, in his particular case of application, it would bring an advantage that outperforms the higher costs. Depending on the result of this consideration he will then select the one or the other implementation of a decoder circuit.

3.6 In this sense, therefore, the subject-matter of Claim 1 is to be regarded as obvious.

3.7 For these reasons, which take full account of the Appellant's arguments as far as they can be accepted, Claim 1 is not allowable and the Appellant's main request must be rejected.

4. The above considerations are apparently not fully applicable to Claim 3.

4.1 The subject-matter of Claim 1 has been found uninventive as the straightforward application of the switching transistors of the IBM citation as controlled, via their bases or gates, from the outputs of the emitter followers, to the "background" prior art of the US citation.

An additional modification of this obvious decoder circuit in the sense of Claim 3 would require an incentive to use, for controlling the bases or gates of the switching transistors, the input signals, rather than the output signals, of the emitter followers, but via level shifting diodes rather than directly, and to provide additional constant current sources.

No such incentive is apparent from either the US or the IBM citation, the introduction of further current sources even appearing as a further step away from the teaching of the US citation.

4.2 Further, the Board considers that this Figure 6 embodiment has an advantage even over the Figure 3 and 4 embodiments in respect of speed of operation for which there is no model in the prior art. This advantage mentioned in the description, is apparently due to the fact that the emitter

followers and the switching transistors are driven in parallel (simultaneously) rather than the latter by the former's output signals (consecutively), as in the IBM citation.

According to the file, this advantage was also the reason for the Primary Examiner not to regard the Figure 6 embodiment as an equivalent to the Figures 3 to 5 embodiments.

4.3 Claim 3 is therefore allowable.

In view of the present prior art situation a two part form according to Rule 29(1) a/b would not appear appropriate.

Only a few corrections in respect of the reference signs are necessary, for instance, because the number of address buffers (1....n) as referenced is inconsistent with the number of decoder line pairs (0...n) as depicted in the figures.

5. The description is also not ready for grant of a patent on the basis of Claim 3.

5.1 An amendment in accordance with Rule 27(1)(d) is necessary on pages 2, 2a and 3 and on pages 6 and 7.

The embodiments described with reference to Figures 3, 4 and 5 must not be referred to as being "in accordance with this invention". If they are not deleted it must be made clear in the description that they concern decoder circuits which are not claimed as such, but only combined with Figure 6, in the sense that figure 6 replaces the corresponding parts of Figures 3 and 4.

It has been accepted (cf. paragraph 2.1) that both alternatives to which Claim 3 refers, i.e. the matrix of diodes as well as the multi-emitter transistor embodiments of the Figure 6 decoder, have a basis in the application as originally filed, more particularly by the dependence of original Claim 4 on all its foregoing original Claims 1-3. Consequently, the particular reference in the description to the "first" example only when the modification shown in Figure 6 is described (page 3, line 21, page 7, lines 15 and 21) is inconsistent with Claim 3 and is regarded as an obvious error which needs correction to the extent that the description should make it clear that the configuration of Figure 6 is applied to that of Figure 4 as well as to that of Figure 3 according to the invention.

5.2 In view of the relevance of the IBM citation (cf. para. 3.1(d), 3.4, 3.5) this document must be cited in the description. An additional amendment of the description in accordance with Rule 27(1)(c) EPC with respect to this citation is absolutely necessary.

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside;

2. The Appellant's main request is rejected;

3. The case is remitted to the first instance with the order to continue the procedure on the basis of

   (a) a single claim, filed as Claim "4" on 1 August 1986 (Part one) and 1 March 1984 (Part two) and renumbered "3" on 21 August 1986, under the proviso that the

inconsistency in the reference signs be eliminated (cf. paragraph 4.3 of the foregoing reasons for this decision);

(b) a description yet to be amended in accordance with Rule 27(1)(d) and Rule 27(1)(c) EPC, as required under paragraph 5 of the foregoing reasons for this decision;

(c) drawings, six sheets as originally filed or amended in accordance with any deletion of embodiments from the description.

The Registrar The Chairman

S. Fabiani P.K.J. van den Berg