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Bezeichnung der Erfindung:
Title of invention:
Titre de l'invention : Semiconductor integrated circuit device

Klassifikation / Classification / Classement : HO1L27/04, HO1L21/76

ENTSCHEIDUNG / DECISION
vom / of / du 19 June 1985

~~Anmelder / Applicant / Demandeur~~ :

Patentinhaber / Proprietor of the patent / Titulaire du brevet : FUJITSU LIMITED

Einsprechender / Opponent / Opposant : TELEFUNKEN electronic GmbH

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Articles 52(1), 56
"Inventive Step"

Leitsatz / Headnote / Sommaire

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Case Number: T 77 / 84

DECISION

of the Technical Board of Appeal 3.4.1

of 19 June 1985

Appellant: (Opponent)
TELEFUNKEN electronic GmbH
Theresienstrasse 2
Postfach 1109
D-7100 Heilbronn

Representative:

Respondent: (Proprietor of the patent)
FUJITSU LIMITED
1015 Kamikodanaka Nakahara-ku
Kawasaki-shi Kanagawa 211
Japan

Representative:
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53/64 Chancery Lane
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Great Britain

Decision under appeal:

Decision of the Opposition Division of the European Patent Office dated 16 January 1984 rejecting the opposition filed against European patent No. 0 008 903 pursuant to Article 102(2) EPC

Composition of the Board:

Chairman: O. Huber
Member: J. Roscoe
Member: P. Ford

SUMMARY OF FACTS AND SUBMISSIONS

I. On European patent application No. 79 301 700.5 filed on 20 August 1979, claiming priority from a Japanese utility model application of 25 August 1978, European patent No. 0 008 903 was granted on 14 April 1982.

II. The grant of the European patent was opposed in due time and form by:

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and revocation of the patent was requested. IEEE Transactions on Electron Devices, June 1977, pages 771 and 772 (document 1), and DE-B-1 564 547 (document 2) were cited to support the allegation of lack of inventive step.

III. By a decision dated 16 January 1984 the opposition was rejected and the patent maintained in unamended form.

IV. On 16 March 1984 the opponent lodged an appeal against this decision with simultaneous payment of the appeal fee. The Statement of Grounds was filed on 15 May 1984. The appellant (opponent) was of the opinion that the subject-matter of Claim 1 was lacking in inventive step in view of the disclosure in document 1 and in a document US-A-3 590 345 (document 3) newly introduced into the proceedings.

V. A letter, a copy of which had also been sent to the patentee, was received from the appellant on 29 May 1985 in which attention was drawn to yet another document US-A-3 878 551 (document 4) in support of his allegation of lack of inventive step.

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VI. On 19 June 1985, at oral proceedings held at the request of the parties, the patentee submitted a new set of six claims and two pages of description (pages 2 and 3).

VII. The appellant (opponent) requested that the decision under appeal be set aside and that the patent be revoked.

The respondent (patentee) requested that the appeal be dismissed and that the patent be maintained on the basis of Claims 1 to 6 as submitted during the oral proceedings, the description of the granted patent with the substitution, for column 1, line 38 to column 2, line 51, of pages 2 and 3 of the text submitted during the oral proceedings, and the figures of the granted patent.

VIII. Claim 1, the only independent claim, reads as follows:

A semiconductor integrated circuit device including a semiconductor substrate (40) of one conduction type, an epitaxial layer (41) of opposite conduction type formed on the substrate (40), a buried layer (42) of opposite conduction type located between the substrate (40) and the epitaxial layer (41), at least one circuit element (45,46,47,48) formed in the epitaxial layer (41) above the buried layer (42), a first isolation region (43) spaced from the buried layer (42) and extending from the surface of the epitaxial layer (41) into the substrate (40), a second shallower isolation region (44) located within the first isolation region (43) and extending from the surface of the epitaxial layer (41) into the buried layer (42), the first and second isolation regions (43,44) completely surrounding at least one circuit element (45,46,47,48), the integrated circuit device being characterised in that the surface of the substrate (40) and hence of the epitaxial layer (41) lie in the (100) crystal plane, in that the first and second isolation regions (43,44) are formed by aniosotripic etching whereby the isolation regions (43,44) both have a V-shaped cross-section, and thus, in spite of their different depths, are formed simultaneously, and in that the V-shaped surface of the second isolation region is entirely covered by electrically insulating material.

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The word "aniosotripic" at the end of line 20 is obviously intended to read "anisotropic".

The representative of the patentee contended that the relevant disclosure in documents 3 and 4 was in substance the same, but document 3 gave a fuller explanation of the role played by the inner P type isolation wall in combating the problem of the lateral parasitic transistor, the collector of which was constituted by the outer wall. This was to replace the parasitic transistor by two series-connected transistors, one of which was turned off by having its emitter (the inner wall) short-circuited to the epitaxial layer, such short-circuiting being an essential feature. This was not how the inner isolation region of the arrangement claimed in the patent in suit worked. There was nothing in either document to suggest that the walls could be replaced by insulating material. Document 4, at column 2, lines 5-20 referred to use of dielectric isolation in the prior art, but pointed out its disadvantage and rejected it in favour of PN isolation in its own solution to the problems of isolation and parasitic transistor action. It thus led away from rather than towards the claimed arrangement.

The technique of forming isolating grooves as disclosed in document 1 and its advantages were admittedly known in the art but the invention resided not in this technique but in the combination of features set out in the claim. This was not obvious and provided substantial advantages in terms of improved isolation, reduced parasitic currents, and increased packing density.

The appellant (opponent) argued that the role of both P type isolation walls in documents 3 and 4 was to block the flow of currents. Various techniques were available in the prior art for doing this and their respective advantages and drawbacks were well known. In any given set of circumstances therefore the skilled person could select those best suited to his requirements. There was therefore nothing inventive in substituting for the different depth P type walls, insulation lined grooves formed by the technique described in document 1, and the advantages achieved were to be expected.

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REASONS FOR THE DECISION

1. The appeal is in accordance with Articles 106 to 108 and Rule 64; it is therefore admissible.

2. The subject-matter of the current version of the claims and description does not extend beyond the content of the application as filed. The requirements of Article 123(2) EPC are therefore met. The claims have also not been amended during the opposition or appeal proceedings in such a way as to extend the protection conferred and thus conform with the requirements of Article 123(3) EPC.

3. After a thorough examination of the documents relied on by the appellant (opponent) in this appeal and in the foregoing opposition proceedings and those cited in the European search report the Board is satisfied that the semiconductor integrated circuit device claimed in Claim 1 is novel. As the appellant has not alleged lack of novelty the Board finds it unnecessary to discuss the matter further here.

4. It therefore remains to be considered whether the subject-matter of Claim 1 involves an inventive step.

4.1 In the description of the patent in suit the subject-matter claimed is generally discussed in relation to and as a development from a type of device described as conventional and shown in Figures 1A to C. In this device a semiconductor circuit element is formed in an epitaxial layer of N type disposed on a P type substrate and is isolated from adjacent elements by an insulation filled groove. An N+ layer buried beneath the element at the interface of the epitaxial layer and substrate terminates short of the groove, and this is said to lead to formation of a parasitic transistor formed by one of the regions of the circuit element acting as emitter, the epitaxial layer as base, and the parts of the substrate interfacing with the epitaxial layer between the end of the buried layer and the groove as collector. Though this transistor is effectively

eliminated in another so-called conventional device, described with reference to Figures 3A and B, by extending the buried layer to the groove, the resulting device provides a structure to which it is difficult to apply a high voltage.

In relation tc these devices it can be deduced from the statement of advantage at column 2, line 34 et seq. of the patent specification that the main problem to which the invention affords a solution is to eliminate the parasitic transistor in the Figure 1 device, while avoiding the disadvantage associated with the Figure 3 devices.

4.2 The documented prior art devices on which the two-part formulation of Claim 1 is now based are those described in documents 3 and 4. It is these which in the Boards' view come closest to the subject-matter of Claim 1 and against which the inventive step has to be judged. Both documents are concerned with eliminating parasitic transistors occurring in semiconductor integrated circuit devices and use virtually identical measures to this end. Certain of the devices described in document 4, in particular those illustrated in Figures 1, 7 and 10, have all the features of the precharacterising part of the claim, as acknowledged by the patentee at the oral proceedings. In the otherwise similar device described in document 3, the isolation regions extend into contact with, but are not said or shown to penetrate, the buried region and substrate respectively. However, the patentee has not suggested and there is nothing in the documents themselves to suggest that this apparent difference is of any functional significance.

In both documents the isolation regions are formed by diffusion and are of semiconductor material of opposite conductivity type to the epitaxial layer. The second (inner) regions are electrically connected to a part of that layer by a metallisation or a conductor acting to short-circuit the intervening PN junction.

4.3 Document 3 explains that when a wall of a material of conductivity type opposite to that of the epitaxial layer is used for isolating discrete elements in a monolithic integrated circuit vertical and lateral parasitic transistors are formed, with one region of an

element functioning as the emitter and the epitaxial layer as the base of both transistors, and the substrate and isolation wall acting as collector of the vertical and lateral parasitic respectively. It is stated that the gain of the vertical parasitic is degenerated by the presence of the buried layer but that the lateral parasitic does not share the beneficial effects of this layer. The further inner wall (second isolation region) is provided to split the lateral parasitic into two transistors connected in series, the second of which is turned off by virtue of having its emitter (the inner wall), which is also the collector of the first transistor, short-circuited to its base, constituted by the epitaxial layer. The document does not directly refer to that part of the substrate within the outer wall not covered by the buried layer as constituting part of the collector of the objectionable lateral parasitic, but does state that the wall is electrically continuous with the substrate, as the equivalent circuit of Figure 3 shows. The Board takes the view, contrary to that held by the patentee, that it would be evident to the skilled person, bearing in mind that the uncovered part of the substrate is closer to the emitter of the parasitics than is at least part and possibly the whole of the outer isolation wall, that this part constitutes part of the collector of the lateral parasitic rendered ineffective by provision of the inner wall, and thus that, even if the wall were absent or replaced by insulating material, the inner wall would still serve to reduce parasitic transistor action.

If this were not evident from document 3, it would be from document 4 in which, in discussing essentially the same arrangement, reference is made throughout to the problem of a parasitic transistor, the collector of which is formed by the substrate (column 1, lines 31-52; column 2, lines 19-23). At column 4, lines 5-12, before any reference is made to provision of the outer isolation region, which is presented as the source of the problem in document 3, it is stated that the regions of the (isolated) element are completely isolated from the substrate both by the P type isolation region 20 (second isolation region), which prevents lateral flow of charge carriers to the substrate, as well as by the N+ interposed (buried) region.

.../...

4.4 Taking the circuit devices of documents 3 and 4 as a starting point, and considering the advantages over them presented by that claimed, the problem to be solved is seen to be to modify the circuits so as to eliminate disadvantages inherent in them. While documents 3 and 4 make no reference to such disadvantages and do not suggest modifications which would lead the skilled person to the claimed device, the Board cannot share the view of the patentee, expressed at the oral proceedings, that the sentence at lines 5-10 of column 2 of document 4 would lead the skilled person away from the use of insulation as isolation. This sentence actually mentions its successful use and rejects it only on cost grounds. The high cost of such isolation has not prevented its use in applications where cost was not the ruling consideration.

4.5 The person skilled in the integrated circuit art is ever aware of the continuing demand, particularly in circuits destined for military and space applications, for an increase in packing density. He is also familiar with the advantages and drawbacks of the different methods of isolation available, and would thus appreciate that the PN junction form of isolation used in the outer walls in the devices of documents 3 and 4 is too demanding of chip space and thus unable to provide optimum packing density. Also that it results in high capacity to substrate, which is undesirable in high frequency applications, and provides less than optimum isolation. Thus, given circumstances where packing density etc. were the main desiderata and cost of secondary importance, he would consider the available alternatives.

4.6 The polyplanar technique, the use of which is described in document 1 and in the articles referred to therein, is known to provide high packing density and would present itself as an alternative for the first isolation region. As explained in the document, this technique, which requires a substrate having a semiconductor surface of 100 crystallographic orientation, employs an anisotropic etchant to produce steep-sided V-section grooves the depth of which is essentially determined by the width of windows in an oxide etching mask. Grooves of different depths can thus be formed simultaneously simply by providing

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appropriately dimensioned windows. After formation of an oxide (thus insulating) layer over the groove walls the grooves are filled with polysilicon and the resulting surface lapped flat.

Since neither document 3 nor 4 stipulates an orientation of the semiconductor surface different than that required by the technique, and the document 1 itself shows a conventional bipolar transistor formed in the 100 surface, the skilled man would not see this requirement as a barrier to use of this technique to replace the PN junction isolation.

4.7 The skilled person, though recognising that the second (inner) semiconductor isolation region used in documents 3 and 4 would overcome the problem of parasitic currents to the substrate subsisting after replacement of the outer isolation region by an oxide-lined V-groove, also knows that it occupies valuable chip space, and is thus motivated to seek a substitute for this also. Having regard to its broad function of preventing lateral flow of charge carriers to the substrate (column 4, lines 9-10 of document 4) and knowing that the essential role of both semiconductor and insulation isolation walls is to block current flow, whether supported by majority or minority carriers, the skilled person is again led to the use of an insulating wall, notwithstanding the fact that the semiconductor wall achieves its effect in the application under consideration by actively collecting rather than passively confining the carriers. That such a wall, of the desired narrowness, could be formed simultaneously with the deeper first isolation region (V-groove) without the need for a further processing stage is evident from document 1.

Under these circumstances it was obvious for a person skilled in the manufacture of integrated circuits to replace both the inner and outer P type isolation walls of the structures in documents 3 and 4 by grooves lined with insulating material simultaneously formed using the etching technique disclosed in document 1.

4.8 Thus the Board concludes that the subject-matter of Claim 1 does not involve an inventive step in the sense of Article 56 EPC. Claim 1 is therefore not allowable under Article 52(1) EPC.

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5. Claims 2 to 6 are formulated as dependent claims, the allowability of which is conditional on that of Claim 1. Furthermore, since the type of circuit element specified in Claim 2 is disclosed in Figure 10 of document 4, and the materials for forming the isolation regions referred to in the remaining claims are conventional, the Board can find no patentable feature in these claims.

O R D E R

For these reasons it is decided that:

The decision of the Opposition Division is set aside and the patent is revoked.

The Registrar	The Chairman
B A Norman	O Huber