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Aktenzeichen / Case Number / N° du recours : T 134/84 - 3.5.1

Anmeldenummer / Filing No / N° de la demande : 79 103 927.4

Veröffentlichungs-Nr. / Publication No / N° de la publication : 0 013 297

Bezeichnung der Erfindung: Latent Image Memory
Title of invention:
Titre de l'invention :

Klassifikation / Classification / Classement : G11C 19/28

ENTSCHEIDUNG / DECISION
vom / of / du 18 July 1988

Anmelder / Applicant / Demandeur : IBM Corporation

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence : Latent memory/IBM

EPÜ / EPC / CBE Art. 56

Schlagwort / Keyword / Mot clé : Inventive step (yes)

Leitsatz / Headnote / Sommaire

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Case Number : T 134/84 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 18 July 1988

Appellant : International Business Machines Corporation
Armonk, N.Y. 10504
USA

Representative : Barth, Carl Otto
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Decision under appeal : Decision of Examining Division 067 of the European Patent Office dated 13 February 1984 refusing European patent application No. 79 103 927.4 pursuant to Article 97(1) EPC

Composition of the Board :

Chairman : J.A.H. van Voorthuizen
Members : P. Ford
P.K. van Henden

Summary of Facts and Submissions

I. European patent application No. 79 103 927.4 filed on 12.10.79 (Publication No. 0 013 297) and claiming a priority of 29.12.78 (US) was refused by a decision of the Examining Division 067 dated 13.02.84. That decision was based on Claims 1-6 submitted on 20.06.83.

II. The reason given for the refusal was that the claimed subject-matter did not involve an inventive step having regard to US-A-3 995 302, US-A-4 040 017, US-A-4 060 738, US-A-4 072 977 and Electronics Letters 13.01.72, pp. 13-14.

III. The Appellant lodged an appeal against this decision on 20.02.84. The appeal fee was paid on the same date. On 23.05.84 the Statement of Grounds was filed.

IV. After a correspondence between the Appellant and the Rapporteur in which the latter set out objections to the then valid claims and drew attention to US-A-3 755 793 which appeared to represent the prior art closest to the invention, the Appellant filed on 05.11.87 an amended set of Claims 1-4 and submitted a revised version of Claim 1 on 23.06.88. The new Claim 1 is in effect the combination of Claims 1, 2 and 6 which were considered by the Examining Division.

V. In the Statement of Grounds and in the course of the further procedure before the Board the Appellant argued essentially that none of the documents cited against the application, taken singly or in combination would give an indication to the person skilled in the art how to arrive at a latent image memory as disclosed in the present application. Although some features apparently similar to

those figuring in the claims might be found in these documents there was nowhere any suggestion which could lead the skilled person in an obvious way to the particular combination of features now claimed. The rejection of the application was therefore considered as being based on an ex post facto analysis.

VI. The Appellant requested the grant of a European patent on the basis of Claim 1 filed on 23.06.88 and Claims 2-4 filed on 05.11.87, said Claim 1 reading as follows:

1. Latent image memory in matrix form having a semiconductor substrate (10) of a first conductivity type covered by a dielectric medium and sets of mutually orthogonal word lines (26 to 48) and bit/sense lines (B/S1; B/S2), enabling selective detection of charge stored in two types of storage cells, which are formed in the substrate (10), which are distinguished by differently doped regions which establish a permanent predetermined pattern of binary information for use of the memory in ROM mode, and having diffusion regions (12, 14, 16) of a second conductivity disposed within said substrate (10), characterized in that each bit/sense line (BS1; B/S2) is connected to all diffusion regions (12, 14, 16) extending along said bit/sense line,

that the storage cells under said bit/sense line (B/S1) between two diffusion regions (12, 14) are formed by abutting impurity regions, each impurity region either consisting of substrate (10) material to form first impurity regions enabling storage of a first amount of charge, or being doped to a different concentration to form a second impurity region (18, 20) enabling storage of a second amount of charge, and

that the impurity regions are covered by a dielectric medium (24) and parts of the conductive word lines (26 to 48) so as to form a charge channel (104) to at least one diffusion region (12, 14, 16) by applying a voltage of a predetermined magnitude to all the word lines between two subsequent diffusion regions,

that a charge is transferred from at least one of the diffusion regions (12, 14, 16) to the impurity regions of the storage cells, that the amount of charge stored in these storage cells is selectively detected by applying a voltage of a predetermined first magnitude to at least some of the word lines (24 to 48) and subsequently decreasing the voltage applied to a selected one of these word lines (24 to 48) at least for a given time interval to a predetermined second magnitude, and that

the charge transfer is detected from the storage cell associated with the selected word line (e.g., 26) and a selected sense line (e.g., B/S1) to at least one of the diffusion regions (e.g. 12, 14) associated with the selected sense line (e.g., B/S1).

Reasons for the Decision

1. The appeal complies with Art. 106 to 108 and Rule 64 EPC and is, therefore, admissible.

2. The general principle on which ROM's are based is to provide at the storage places in an array (either for read-out in serial form or capable of random access) elements having each one of two possible conditions. These conditions can be permanent as in a pure ROM or semi-permanent as in an EPROM (also called non-volatile RAM). E.g. transistors may be used of which certain electrodes

are disconnected or short circuited. Another example is provided by US-A-3 755 793 which describes a memory in matrix form having a semi-conductor substrate covered by a dielectric medium and sets of mutually orthogonal word and bit lines, enabling selective detection of charge stored in the storage cells. Two types of storage cells are formed in the substrate, which establish a permanent predetermined pattern of binary information for use of the memory in the ROM mode.

US-A-4 072 977 discloses a serial read-out memory in which ROM coding may be provided by different doping of the storage areas (page 5, left column, lines 55-59). In the ROM's according to both documents CCD structures are used and the way of doping differs from the one used in the present application.

3. US-A-4 014 036 and US-A-4 060 738 describe RAM structures using CCD's in which regions having different dopings are used which thereby exhibit different threshold voltages.

4. A general trend in semi-conductor memories being towards high density charge storage systems, the problem of constructing a ROM being able to be addressed in random fashion and having a high density of storage cells must be considered as presenting itself in an obvious manner to the person skilled in the art. it must also be regarded as clear to that person that CCD type cells, which need at least two different regions (source, gate, store) could not readily provide an optimal density of cells and that cells having only a single region looked more promising.

5. The article in Electronic Letters, 1972, page 13/14 describes a non-volatile electric store comprising a source and a drain and a number of gate electrodes which act as separate memory elements. By altering the threshold

voltages a binary pattern can be written in. It is pointed out that, in a matrix configuration, these devices offer the possibility of a very high density of elements in a simple interconnection pattern. Due to the close spacing of the gate electrodes, which function analogous to the word lines in the present application, a continuous channel can be obtained between source and drain, which is used to read out information by applying suitable voltages to the gates. The manner of reading out is different, however, from that provided in the present application, in that no charge transfer takes place.

6. Finally US-A-4 040 017 describes a high-density RAM arrangement having a plurality of inversion storage capacitors. A continuous channel permitting charge transfer from diffusion regions to the capacitors and vice versa may be formed due to the fact that each word line contacts the dielectric/semi-conductor structure between each pair of neighbouring bit lines. The storage cells do not exhibit different threshold voltages and moreover the memory array is word-organised so that the way in which the information is read out, although employing a charge transfer mechanism, is different from that according to the present application.

7. The further documents cited in the description are considered to be still further removed from the invention and need, therefore, not be discussed.

8. In view of the foregoing analysis of the documents constituting the prior art the Board has come to the conclusion that the said prior art could not suggest to the person skilled in the art the particular charge transfer and detection mechanism which in combination with further features related thereto constitutes the subject-matter of the present Claim 1, which therefore, must be held allowable.

9. Dependent Claims 2-4 describe particular embodiments of the invention and are not open to objections.

10. The amendments to the description submitted on 05.11.87 take properly account of the prior art and of the terms of the claims in their present form. They are not open to objection.

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a European patent on the basis of the following documents:

   (a) Claim 1 as filed on 23.06.88 and Claims 2-4 as filed on 05.11.87,

   (b) Description as amended on 05.11.87

   (c) Drawings as originally filed.

The Registrar The Chairman

S. Fabiani J.A.H. van Voorthuizen

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