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Bezeichnung der Erfindung: Method of increasing the speed of a computer system  
Title of invention: and a computer system for high speed operation  
Titre de l'invention :

Klassifikation / Classification / Classement : G06F 13/00

### ENTSCHEIDUNG / DECISION

vom / of / du 7 March 1990

Anmelder / Applicant / Demandeur : IBM Corporation

Patentinhaber / Proprietor of the patent /  
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPU / EPC / CBE Article 56

Schlagwort / Keyword / Mot clé : "Inventive step (yes) - modification  
unobvious"

Leitsatz / Headnote / Sommaire



Case Number : T 239/84 - 3.5.1

**D E C I S I O N**  
of the Technical Board of Appeal  
of 7 March 1990

**Appellant :** International Business Machines Corporation  
Armonk, New York 10504  
USA

**Representative :** Ahlman, Bertel  
IBM Svenska AB  
Intellectual Property Department  
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**Decision under appeal :** Decision of Examining Division 065  
dated 15 May 1984 refusing European  
patent application No. 80 102 987.7  
pursuant to Article 97(1) EPC

**Composition of the Board :**

**Chairman :** P.K.J. van den Berg  
**Members :** W.B. Oettinger  
P. Ford

## Summary of Facts and Submissions

- I. European patent application No. 80 102 987.7, filed on 29 May 1980, claiming a priority of 29 June 1979 and published under No. 21 097, was refused by a decision of Examining Division 2.2.01.065 dated 15 May 1984.

The reason given for the refusal was that the subject-matter of method Claim 1 filed on 13 August 1983 and of system Claim 7 filed on 25 March 1983 did not involve an inventive step having regard to the prior art disclosed in US-A-3 685 020.

The same conclusion was drawn for dependent method Claims 2 and 3-6, filed on 13 August 1983 and 25 March 1983, respectively.

- II. On 20 June 1984, the Applicant lodged an appeal repugning that decision in its entirety and paid the appeal fee.

A Statement of Grounds and a new system Claim 7 were filed by the Appellant on 1 September 1984.

- III. In response to communications from the Board, in which

- some doubts to the proper formulation of the independent claims were expressed,
- reference was made to the "Encyclopedia of Computer Science" by A. Ralston, First Edition 1976, pages 11-12, 133-136 and 191-192, as a standard book showing possibly more clearly than the cited US patent specification the relevant background art possibly more clearly than the cited US patent specification, and

- the Appellant was invited to further specify his argumentation in support of an inventive step,

the Appellant filed, on 22 January 1990, new Claims 1-6.

In his replies, he stressed his opinion that from none of the prior art documents is it obvious to use address parameters such as base and displacement directly in an associative search for a data word access. The gist of the invention is the avoidance of the conventional address generation phase for obtaining an effective address and the saving of such steps results in an increased speed of the computer.

The independent claims read as follows:

"1. A computer system of increased speed comprising a memory cache (2), a processing unit (1) including general registers (4), used for address relocation or modification or as operand recipients, and an arithmetic logic unit (5), the processing unit generating instructions (6) for data access, said instructions including address parameters representing base (7) and displacement (8) information, a plurality of implicit registers (9) in an associative memory (3) attached to the processing unit, an address word (11) being provided for each implicit register for register data (10) identification purposes, means transferring a command signal (104) generated in the processing unit (1) to the associative memory (3) to start an address compare operation and means transferring upon occurrence of a match in the compare operation in one of the registers, the data (10, 340, 342) stored in that register and a "data valid" signal (110) generated in the associative memory (3) to the processing unit (1), the processing unit further

commencing to generate an address for obtaining said data from the memory cache (2) when said instruction is generated, and the "data valid" signal (110) transferred to the processing unit with the data functioning to abort the address generation, and in the absence of a match in the compare operation in any of the implicit registers (9), no "data valid" signal (110) being transferred to the processing unit and the address generation continuing to produce an address, characterized by means (386, 390, 377, 382) transferring the base and displacement parameter words contained in an instruction in the processing unit to the associative memory and means (326, 330) comparing directly the transferred base and displacement parameter words with those contained in the address words of each of the implicit registers.

6. A method of operating a computer system comprising a memory cache (2), a processing unit (1) including general registers (4), used for address relocation or modification or as operand recipients, and an arithmetic logic unit (5), wherein the processing unit generates instructions (6) for data access, said instructions including address parameters representing base (7) and displacement (8) information, the method including attaching a plurality of implicit registers (9) in an associative memory (3) to the processing unit and providing an address word (11) for each implicit register for register data (10) identification purposes, and wherein a command signal (104) generated in the processing unit (1) is transferred to the associative memory (3) to start an address compare operation, whereby, upon occurrence of a match in the compare operation in one of the registers, the data (10, 340, 342) stored in that register and a "data valid" signal (110) generated in

the associative memory (3) are transferred to the processing unit (1) and the processing unit further commences to generate an address for obtaining said data from the memory cache (2) when said instruction is generated, and the "data valid" signal (110) transferred to the processing unit with the data functions to abort the address generation, and whereby, in absence of a match in the compare operation in any of the implicit registers (9), no "data valid" signal (110) is transferred to the processing unit and the address generation continues to produce an address, characterized by causing the base and displacement parameter words contained in an instruction in the processing unit to be transferred to the associative memory and to be compared directly with base and displacement parameter words contained in the address words of each of the implicit registers."

IV. (a) From the Appellant's submissions it follows that he requests that the decision under appeal be set aside and a patent be granted on the basis of the following application documents:

- description pages 1-9 and 11-24 as published with "the content of" inserted at the beginning of line 31 on page 3 as requested on 8 November 1982,  
page 10 filed on 8 November 1982;
- Claims 1-6 filed on 22 January 1990;
- drawings, sheets 1-12 as published.

(b) According to his reply filed on 22 January 1990, he leaves it to the Board to decide whether the expression

"such as" should be re-inserted or not in Claims 1 and 6 instead of the expression "representing" suggested by the Board.

### Reasons for the Decision

1. The appeal is admissible.
2. There are no formal objections to the amendments made to the claims as on file.

More specifically, Claim 1 can be derived, as to its structural features, from the original Claim 9 and, as to its functional features, from Claims 3 and 4 in conjunction with the claims from which they are dependent, or from the description.

Claim 6 only defines a method of operating the system claimed in Claim 1 without introducing any additional feature.

3. Referring to the wording of Claims 1 and 6, it is clear that none of the prior art documents on file discloses either the claimed system or its operation:
  - 3.1 The Ralston citation discloses (on pages 191-192) that the speed of a computer system is increased by interposing a cache memory between its main memory and the CPU. To this end, a plurality of implicit registers in an associative memory (see also pages 133-136) are attached to the CPU. The search in the cache for the next word is made by comparing the target word address with addresses stored in the associative memory, the result of a match being the location in the cache of the desired word and no match initiating an access to the main storage (page 192, second paragraph).

According to Ralston (page 11, right-hand column and page 12, Figure 2), the address part of the instructions generated by a processing unit could generally comprise address parameters such as base and displacement information.

In this case, the comparison between the target word address parameters and the addresses stored in the associative memory is, according to Ralston, an indirect comparison in that the transferred base and displacement parameter information is first added (page 12, Figure 2) to generate an effective address word (page 11, right-hand column) for achieving an address word which can be compared with the address words of the implicit registers.

- 3.2 The claimed invention differs from this by the feature that the transferred base and displacement parameter words are directly compared with corresponding base and displacement words comprised in the address words of the implicit registers, with no effective address word being generated.
- 3.3 Since also no other prior art document on file discloses this feature, the subject-matter of Claims 1 and 6 is novel.

This was also the opinion of the Examining Division as expressed in the decision under appeal for the subject-matter of, in substance, similar claims.

4. It still remains to be examined whether the claimed invention involves an inventive step.

Apparently, this question reduces to the simpler question whether it is obvious from any of the prior art documents

not to have an effective address generated by adding the base and displacement parameters but to submit these parameters to a direct comparison with corresponding parameters comprised in the address words of the implicit registers.

In the opinion of the Board, this is not the case for the following reasons and the subject-matter of Claims 1 and 6 is therefore deemed unobvious:

- 4.1 From Ralston, it can only be derived that an effective address is generated before the comparison is made, as said before (3.1).

Nothing in Ralston pointing to another possibility, the ordinary skilled person will have no reason to search for such another possibility.

- 4.2 Such a reason can also not be derived from any other prior art document on file.

The US patent specification discloses, in columns 11-12 and Figure 4, a compound memory (51) comprised of an associative array (2) and a random access array (1). The high order bits (on lines 4) of an effective address (on 77) generated by the processor are compared with an entry in the associative memory (2) and, upon a match, select lines (15) are energized. The low order bits (on 34) of the effective address are used (in 7) for decoding the address words on the energized select lines, thus selecting a particular information block in the random access array (1) for read-out or write-in purposes.

In column 13 and Figure 6, a compound memory for address transformation (program relocation), similarly comprised of an associative array (102) and a random access array (101),

is disclosed. Again, the high order bits (on lines 104) of the effective address are used as an input to the associative array but the low order address bus (134) and corresponding sub-selection (in 107) in the random access array is typically not employed. The actual address transformed from the effective address (on 104) is supplied by an output data register (133) of the random access array. The transformation compound memory of Figure 6 can thus be employed in conjunction with the Figure 4 system.

Alternatively, it can be employed alone as the main memory (68) of that system. In this case, the low order address bits (on 134) are used as in the compound memory (51) of Figure 4.

- 4.3 In any case, even if the "effective address" (column 13, lines 9-10), or rather its high order bits, on the input address bus (104) is regarded as a "base" address parameter, it is not seen that a similar use is made, in the associative array, of the low order address bits, interpretable as a "displacement" parameter.

Either no use at all is made of them or they are used in the decoder (107) of the random access array (101), which is not an (implicit register) part of the associative memory (102), of the transformation compound memory (Figure 6) in the same way as in the decoder (7) of the random access array (1) of the buffer compound memory (51) of Figure 4.

- 4.4 For this reason, the Board considers that the US patent specification does not suggest to modify a system employing, as presupposed by the present claims in the sense of the Ralston citation, implicit registers in an associative memory, by the feature that, instead of comparing the effective address (generated by adding base

and displacement), contained in program instructions, the base and displacement parameters as such are directly compared with corresponding base and displacement parameters contained in the address words of the implicit registers in the associative memory.

- 4.5 With hindsight, the claimed direct comparison between the transferred base and displacement parameters and corresponding parameters comprised in the address words of the implicit registers might appear equivalent to the generation of an effective address word and its comparison with the address words of the implicit registers according to the prior art (Ralston).

It is, however, to be noted that the application teaches that the claimed parameter comparison is made for the particular reason that it speeds up the data access of the computer system still further than the mere use of a cache memory.

This submission appearing correct, the claimed solution cannot be said to be equivalent to the prior art.

Had it been so obvious that the speed of the computer system can be further increased in this way, it could have been expected that Ralston or another prior art document would refer to this possibility, high computer speed being a general objective in the art and also being on the basis of the US patent specification.

5. It is noted that the Examining Division did not raise the question whether the subject-matter of the application might be excluded from patentability by Article 52(2) and (3) EPC.

The Board considers that the Examining Division was right not to raise it. The claimed invention is concerned with internal functions of the computer system and has clearly a technical effect.

6. The Board has considered the question whether another objection might arise against method Claim 6.

Claim 1 defines, as is admissible, most of the technical features of the system in functional terms.

Claim 6 is directed to a method of operating this system, the latter again being defined by its functional features. Thus, Claim 6 only defines what happens in the system when it is being operated, i.e. used.

Nevertheless, although Claim 6 contains no additional or differing feature, its scope of protection would, as in other cases of different categories, e.g. product and use (Rule 30 EPC), not necessarily be the same as that of Claim 1.

For this reason, the Board accepts that Claim 6 is neither clearly superfluous nor objectionable for any other formal reason.

7. Although not formulated as a request, the Appellant would prefer that in both claims the expression "representing", suggested by the Board, be re-amended to "such as". The Board wishes to set out its reasons for not doing so:

As rightly pointed out by the Appellant, there may be other parameter words in an instruction in addition to base and displacement parameters. However, the original expression "such as" in the preamble of the claims appeared

inconsistent with the fact that the characterising features deal only with base and displacement parameter words.

The suggested amendment to "representing" removes this inconsistency without excluding the aforementioned possibility that there may be additional parameter words in an instruction.

#### Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.
2. The case is remitted to the first instance with the order to grant a patent on the basis of the application documents cited under foregoing item IV(a).

The Registrar:

The Chairman:

S. Fabiani

P.K.J. van den Berg