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Bezeichnung der Erfindung:
Title of invention: Integrated semiconductor circuit chip
Titre de l'invention :

Klassifikation / Classification / Classement : H 01 L 31/14, H 04 B 9/00

ENTSCHEIDUNG / DECISION
vom / of / du 11 January 1988

Anmelder / Applicant / Demandeur : IBM, Armonk (US)

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE 56 EPC

Kennwort / Keyword / Mot clé : Inventive step (yes)

Leitsatz / Headnote / Sommaire

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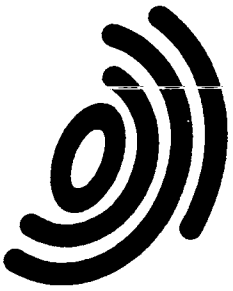

Case Number : T 257/84

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 11 January 1988

Appellant : International Business Machines Corporation
Armonk, N.Y. 10504
USA

Representative : Bravi, Alfredo
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Decision under appeal : Decision of Examining Division 048 of the European Patent Office dated 17 May 1984 refusing European patent application No. 80 102 572.7 pursuant to Article 97(1) EPC

Composition of the Board :

Chairman : K. Lederer
Members : E. Turrini
P. Ford

Summary of Facts and Submissions

I. European patent application No. 80 102 572.7, (publication number 0 019 234) claiming priority of a US application filed on 21 May 1979, was refused by decision of the Examining Division. That decision was based on Claims 1 and 2 filed on 4 July 1983.

II. The reasons given for the refusal were that:

(1) the subject-matter of Claim 1 did not involve an inventive step having regard to GB-A-1 137 915 (D1), IBM-Technical Disclosure Bulletin, Volume 15, No. 9, February 1973, pages 2760 and 2761 (D2) and Applied Physics Letters, Volume 34, No. 7, April 1979, pages 430 and 431 (D3) (Articles 52(1), 56 EPC);

(2) the subject-matter of Claim 2 contained subject-matter extending beyond the content of the application as filed (Article 123(2) EPC).

III. The appellant filed a notice of appeal. A statement setting out the grounds of appeal accompanied by new Claims 1 and 2.

IV. Following a communication on behalf of the Board of Appeal, the appellant filed additional arguments in favour of the existence of inventive step and, on 3 December 1987 a letter requesting that the decision of the Examining Division be set aside and a European patent granted on the basis of a new single claim filed with this letter.

V. Current claim reads as follows:
"Integrated semiconductor circuit chip including photoelectric receiver input means (4) receiving signals from the outside of the chip and operable to convert optical signals into electrical signals, processing means comprising an array of electric circuit components (9, 10) and being operable to process electrical signals supplied thereto by said input means (4), and electrooptic driver output means (3) transmitting signals to the outside of the chip derived from the electrical signals supplied thereto by said processing means and operable to convert electrical signals into optical signals, the processing means, the input means (4) and the output means (3) being physically separated from each other, characterised in that said chip is a large scale monolithically integrated chip using a material having both high carrier mobility and good electrooptic and optoelectric conversion properties, and in that said chip is provided with at least two optical fibers (5, 6), one (6) of them being adjacent to and in optical coupling with the input means (4) and the other (5) with the output means (3), so as to optically connect the chip, when incorporated in a multichip system with other two chips of the system".

VI. The appellant argues essentially as follows:

The invention solves two main problems, i.e. the "off-chip delay" which has been a severe limitation in the speed of processing informations in multi-chip systems, and the high power requirements of the conventional drivers which transmit the electrical signals out of the chip. None of the prior art cited documents alone or in combination suggests any structure for solving the problem underlying the invention.

In particular, D1 refers to a chip, wherein the light emitter is not and cannot be (because the silicon substrate

is not a light source) monolithically integrated. Moreover, in that document there is no indication of the possible utilisation of optical fibres connected with the input and output means. The chip of D1 is clearly confined in the area of the display devices or of the image processing devices.

Documents D2, D3 and FR-A-2 019 059 (D4) are in the area of the "integrated optical circuits" (IOC's), whereby light is generated, guided through a circuit and eventually detected.

The devices described in documents D1 to D4 are not concerned with the propagation delay and power dissipation problems solved by the invention.

Thus, although the elements of the invention are known per se, a skilled man would not obtain the invention from the disclosures of the cited documents.

VII. To clarify some concepts and the technical background of the invention, the appellant filed excerpts from textbooks and dictionaries as well as a technical opinion given by an expert.

Reasons for the Decision

1. The appeal is admissible.

2. There is no objection to the present application on formal grounds, since it is adequately supported by the specification as originally filed (Article 123(2) EPC).

More specifically, the present claim includes the features of original Claim 1 (the expression of the present claim "monolithically integrated chip" is supported by the

wording of original Claim 1 "Semiconductor integrated circuit structure comprising a substrate of a semiconductor material, circuit components formed on said substrate and employing said semiconductor material"; ...."said converters being formed on said substrate and employing said semiconductor material") and other features disclosed in the original description (the expression of the present claim "processing means comprising an array of electric circuit components and being operable to process ..." is supported by the original description, page 4, first paragraph; the expression "large scale ..." of the present claim is supported by the description, page 2, third paragraph; the expression of the present claim "both high carrier mobility and good opto-electric conversion properties" is supported by the original description, page 3, first paragraph; the last part of the present claim starting from "said chip is provided ..." is supported by the description, page 2, first and fourth paragraphs, page 3, third and fourth paragraphs and page 4, first paragraph).

The Art. 123(2) objection raised by the Examining Division has been met by deletion of the then valid Claim 2.

3. Novelty.

3.1 Document D1 (figure and corresponding description) refers to an integrated semiconductor chip (figure) including:

- photoelectric receiver input means (3) (page 1, lines 74 to 77) receiving signals from the outside of the chip and operable to convert optical into electrical signals;

- processing means (2) (page 1, lines 69 to 71; page 2, lines 31 to 36) comprising an array of electric circuit

components and being operable to process electrical signals supplied thereto by said input means (3);

- electrooptic driver output means (5) (page 1, lines 84 to 90) transmitting signals to the outside of the chip derived from the electrical signals supplied thereto by said processing means and operable to convert electrical signals into optical signals.

The above-mentioned features of the semiconductor chip of D1 correspond to the subject-matter of the preamble of the claim. However, the semiconductor chip of D1 does not comprise any feature of the characterising portion of the claim. In particular, said chip is not large scale and monolithically integrated (page 1, lines 80 to 90), there is no mention of the use of optical fibres and of the fact that it is part of a multi-chip system and the semiconductor is silicon, i.e. it does not have the capability of exhibiting both electroluminescence properties and high carrier mobility.

3.2 Document D2 describes a monolithically integrated semiconductor chip (10) (for an optical data transmission system) comprising a photoelectric receiver means (C) and an electrooptic driver means (A) provided with at least two optical fibres (F) so as to connect the chip, when incorporated in a multi-chip system (e.g. a closed loop as in Fig. 2), with two other chips of the system. The semiconductor is gallium arsenide, i.e. presenting both high carrier mobility and good opto-electronic conversion properties.

Contrary to the subject-matter of the claim, D2 refers to an "integrated optical circuit" (IOC), i.e. the light is guided around the chip and electrical processing means are

not mentioned. Moreover, the circuit is not defined as "large scale".

3.3 Document D3 (figure 1 and corresponding description) refers to a monolithically integrated semiconductor chip made of gallium arsenide, input means (to control the MESFET), receiving signals from the outside of the chip, processing means (modulation of laser current by the MESFET) operable to process electrical signals supplied thereto by said input means and electrooptic driver output means (the laser) transmitting signals to the outside of the chip derived from the electrical signals supplied thereto by said processing means and operable to convert electrical signals into optical signals. Optical fibres coupled to the output means are also foreseen (page 430, left column, first three lines).

Contrary to the subject-matter of the claim, in the device of D3 the input means are purely electrical means, the processing means does not comprise an array of electric circuit components, the chip is not large scale integrated and is not connected with other chips of a multi-chip system.

3.4 Document D4 (figures 5 to 8 and description, pages 15 to 19) refers to a monolithically integrated semiconductor circuit chip comprising photoelectric receiver means (371', 372', 47, 47') and electrooptic driver means (33-34, 33'-34', 44-44', 45-45').

Contrary to the subject-matter of the claim, D4 refers to an "integrated optic circuit" with the addition of integrated electrical connections in the chip (37,37'; 46-46').

Moreover, the presence of processing means and of optical fibres for optically coupling the input and output means with other external units is not mentioned and the features of a semiconductor presenting both high carrier mobility and good optoelectronic conversion properties are not disclosed.

3.5 US-A-4 041 475 (D5), cited by the applicant, describes a memory system in which communication to and from the memory cells is effected by optical means. Thus, the system comprises electrooptic input-output means (132, 138, 140) and processing means (128, 136) connected to the input-output means. Said system is connected with other devices (16, 18).

Contrary to the subject-matter of the claim, the system of D5 is not an integrated semiconductor circuit and is not connected via optical fibres with other chips of a multi-chip system.

3.6 US-A-4 065 729 is not relevant with respect to the present application in spite of the formal similarities with the present invention, due to the fact that is in another technical field (it refers to an optical repeater). The document "A monolithically integrated optical repeater", Applied Physics Letters, Volume 35, No. 10, 15 November 1979, New York, US, does not form part of the state of the art due to the fact that the priority has rightly been claimed and covers the whole subject-matter of the application in suit.

3.7 For the above reasons the subject-matter of the claim is deemed to be novel within the meaning of Article 54 EPC.

4. Inventive step.

4.1 The claim is based, as before outlined, on D1, which is, in the Board's opinion, the nearest prior art. Starting from the disclosure of this document, a first problem to be solved is to simplify the chip rendering it more compact and a second problem is to reduce the "off-chip delay" in the communication between the claimed chip and other chips, when the chip is incorporated in a multi-chip system.

4.2 The two problems are solved by the features of the characterising portion of Claim 1.

4.3 The identification of said first problem is per se not inventive, since it is a common goal in the integrated chip electronics field to reduce the size of a chip and simplify its construction.

4.4 As far as the solution of the first problem is concerned, a man skilled in the art would as a matter of course try to transform a chip as known from D1 in a monolithic chip by employing the same semiconductor material for realising the input and output and the processing means. He would easily recognise that silicon, the substrate material of the known chip, would not allow the integration of the output means, as silicon is not suitable as a light source. However, D2 and D3 would suggest the use of gallium arsenide as substrate presenting both high carrier mobility and good opto-electronic conversion properties, since the chip of D2 comprises opto-electric and electro-optic means and the chip of D3 comprises electro-optic and processing means. The skilled man would, therefore, modify the semiconductor chip of D1 on the lines before-mentioned so as to obtain a fully monolithic integrated chip. He would also increase the component density utilising the well known "large scale integrated circuit techniques".

In this way the skilled man would solve without inventive activity the first problem.

4.5 As far as the second problem is concerned, the Board of Appeal is of the opinion that it is not possible to take it into consideration separately from its solution. Indeed, the identification of the second problem includes already, to some extent, the solution, due to the fact that the skilled man as first step should have to recognise that the chip with its optical input and output would be suitable for connection with other chips and that an optical connection would substantially reduce the "off-chip delay" in a multi-chip system. Once the skilled man would have recognised this, he should, as second step, merely effect the optical connection by means of optical fibres and he would then obtain the invention as claimed.

While the second step is considered routine for the skilled man, because the optical fibres are well known to be suited as optical paths due to their characteristic of keeping the light losses quite low (a hint at this solution can e.g. be found in document D3, first paragraph), the first step is considered not obvious.

Indeed, documents D1, D2 and D3 do not even hint at input-output communication between chips of a multi-chip system. Thus, there is no reason for the skilled man to utilise the chip described in part 4.4. of the present decision in a multi-chip system in order to reduce the propagation delay time by means of optical communication. It is true that document D5 raises the problem of reducing the propagation delay time in the input and output of a computer memory system (column 1 "Background of the invention") and suggest a solution by means of optical communication (columns 1 and 2, "Summary of the invention"). However, the skilled man would not see any linkage between the problem and solution

referred to in document D5 and the chip described in part 4.4 of this decision, the purpose of the latter chip being totally different (compactness and simplification of chips).

The other cited documents do not help to identify or solve the second problem before-mentioned.

Thus, the subject-matter of Claim 1 is considered to involve an inventive step within the meaning of Article 56 EPC and Claim 1 is, therefore, admissible under Article 52(1) EPC.

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a European patent on the basis of the following documents:

2.1 Description: as filed on 27 October 1987.

2.2 Unique claim as filed on 3 December 1987.

2.3 Drawing: Sheet 1/1 as originally filed.

The Registrar

The Chairman

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