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Bezeichnung der Erfindung:
Title of invention:
Titre de l'invention : Arrangement for bidirectional information transfer on a single direction bus

Klassifikation / Classification / Classement : G06F 3/02

ENTSCHEIDUNG / DECISION

vom / of / du 5 December 1989

Anmelder / Applicant / Demandeur : IBM Corporation

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Article 56 EPC

Schlagwort / Keyword / Mot clé : Inventive step (no)

Leitsatz / Headnote / Sommaire

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Case Number : T 282/85 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal
of 5 December 1989

Appellant : International Business Machines Corporation
Armonk
New York 10504
USA

Representative : BONNEAU Gerard
COMPAGNIE IBM FRANCE
Département de Propriété Industrielle
F-06610 - La Gaude

Decision under appeal : Decision of Examining Division 065 of the European Patent Office dated 27 June 1985 refusing European patent application No. 81 103 623.5 pursuant to Article 97(1) EPC

Composition of the Board :

Chairman : P.K.J. van den Berg
Members : J.A.H. van Voorthuizen
F. Benussi

Summary of Facts and Submissions

I. European patent application No. 81 103 623.5 (publication No. 0 042 952) claiming a priority of 27.06.80 (U.S.A.) was refused by decision of Examining Division 2.2.01.065 dated 27.06.85.

II. That decision was based on Claims 1-5 filed on 18.10.84 on the ground that the subject-matter of these claims was not considered to involve an inventive step with respect to the prior art disclosed in DE-A-2 407 599 (doc. 1) and IBM Technical Disclosure Bulletin, January 1977, pages 2840-2844 (doc. 3).

III. The Appellant lodged a Notice of Appeal on 08.08.85 and paid the relative fee on the same date. The Statement of Grounds was filed on 22.10.85.

IV. In communications dated 2.12.87 and 23.02.89, the Rapporteur further drew the Appellant's attention to US-A-3 740 725 (doc. 2) and FR-A-2 319 157 (doc. 5), cited in the search report, and expressed doubts as to the presence of inventive step in the subject-matter of the application.

V. On 06.08.88 the Appellant filed a revised set of Claims 1-8, of which Claim 1 reads as follows:

1. Arrangement for bidirectional digital data transfer between a central processing unit (1) for processing said digital data and for supplying digital data output signals indicative of status information in response to digital data input signal, and an operator console (3) externally located from said central processing unit, being activatable for providing a predetermined number

of said digital data input signals to said central processing unit, and further comprising a selectively operable advisory unit being responsive to said digital data output signals from said central processing unit; said arrangement comprising:

interface means (2) interconnecting said central processing unit and said operator console, for transferring digital data therebetween,

reference means in said central processing unit providing to said operator console through said interface means a count sequence of reference digital data signals corresponding to said predetermined number of digital data input signals, said reference means comprising a recirculating binary counter (11) which is continually incremented at a clock rate sufficiently high to provide said reference data signals enabling the sampling of any information input at said operator console, and

a comparator (12) in said operator console operable to compare said count sequence of digital data signals received from said recirculating counter, said comparator having a single signal line (15) connected to said central processing unit, which becomes active when said reference data signals are identical to said digital data input signals;

said arrangement being characterized in that

said interface means (2) comprises a single undirectional bus (13) for normally transferring digital data from said central processing unit to said operator console, operable in a first mode for interconnecting said reference means to operator

console for transfer of said reference data signals to said comparator and operable in a second mode for interconnecting said central processing unit to said advisory unit for transfer of said digital data output signals to said operator console thereby making said bus unavailable for transfer of digital data in an input direction from said operator console to said central processing unit, and

said comparator sends, when said reference signals are identical to said digital input signals, a signal on said single signal line for stopping said recirculating counter so that its contents can be read by said central processing unit as said digital data input signals provided by said operator console, thereby accomplishing transfer of said digital data input signals from said operator console to said central processing unit and transfer of said digital data output signals from said central processing unit to said operator console by utilizing only said undirectional bus and said single signal line.

Claims 2-8 are dependent on Claim 1.

VI. Oral proceedings were held on 05.12.89 during which the Appellant amended Claim 1 in that in line 5 after "signals" is added: "from a keyboard activated by an operator", in lines 9 and 10 the phrase "further ... unit" is deleted, lines 20-24 are transferred to the characterising part and "advisory unit" in line 8 of the characterising part is replaced by "operator console". He requested the grant of a European patent on the basis of the so amended Claim 1 and Claims 2-8 as filed on 06.08.88.

VII. The Appellant's submissions can be summarised as follows:

Doc. 1 may be considered as the prior art closest to the invention as it shows an arrangement for transferring the states of switches to a CPU. The arrangement comprises reference means in the form of an address generator, a comparator and a single signal line which becomes active when an activated switch is detected. The switches serve to choose sub-programmes to a program which is run on the CPU and when an activated switch is detected the CPU is instructed to carry out the sub-program corresponding to the address of that switch..

It can be seen, therefore, that the problem solved by doc. 1 is entirely different from that solved by the invention.

The problem of the invention is to reduce the total number of signal cables by using a single unidirectional bus for accomplishing transfer of data in either of two directions between a processor and the associated operator console. In one mode the bus is used as a data bus to operate display indicators, and in a second mode the bus is used to determine the status of the keyboard.

The difference between the problems solved by the invention and the prior art results in several major differences between the features involved.

In order to determine, according to the invention, the status of the keyboard and to detect when a key is depressed by the operator, it is necessary to scan systematically all the keys of the keyboard. A recirculating binary counter is a convenient device for the purpose. This is not necessary in the prior art system.

The known device calls either one or more predetermined switches systematically or the whole of these switches one after the other in accordance with a standard call program. For this reason, the address generator is a programmable memory.

The recirculating counter is continually incremented at a clock rate sufficiently high to provide reference signals enabling the sampling of any information entered at the console. On the contrary, the address generator of the prior art system is activated only when it is necessary to check the activation of a switch associated with a part of program to be executed.

As a consequence, the recirculating counter of the invention is stopped when the reference signals match the signals provided by the console. Though there is no mention of this point in the DE document, it is clear that such a step is not necessary with the memory which is activated only when the CPU has to check the activation of a switch.

Likewise, the output signal line of the application is used to stop the recirculating counter, whereas the line of the DE document is used to transmit a signal to the computer which employs the address signal to execute the corresponding part of the program.

In view of these differences between the prior art and the invention, the Appellant considers that the skilled person could not have come to the claimed invention without inventive activity. Neither could the other documents cited have led him to the invention.

Reasons for the Decision

1. The appeal is admissible.

2. The Appellant considers doc. 1 as being the prior art closest to the invention because the arrangement disclosed therein comprises some of the means which form part of the arrangement according to Claim 1. While it would not appear to be excluded to start from this document as prior art, the Board prefers to consider doc. 2 as the prior art coming nearest to the application as this document relates to an arrangement of the same basic kind and used for the same purpose as that of the application, i.e. an arrangement for bidirectional digital data transfer between a central processing unit (CPU) and an operator console located externally from the CPU and which comprises a keyboard.

3. In the arrangement known from doc. 2, each console is provided with a data buffer storing digital data signals representing the position of depressed keys in the keyboard, which signals are inputted to the CPU. To this end the buffers are sampled in turn by a multiplexer in the CPU via a first set of conductors. Data indicative of status information to which the console is responsive is supplied by the CPU to the consoles via a second set of conductors.

4. This means that the bus connecting each console to the CPU must have a relatively high number of conductors. The present invention is concerned with the problem of reducing the total number of signal conductors. Generally, however, the person skilled in the art wishes to reduce the number of conductors in a bus arrangement and equally the number of pins required to connect a CPU chip to peripheral equipment. Therefore, it has become usual e.g. to use the same conductors and pins for input and output purposes. The problem which the invention aims to solve can thus not be considered as contributing to an inventive step.

The invention proposes to solve the said problem by providing means as specified in Claim 1 permitting a unidirectional bus to be used as a quasi-bidirectional bus so that in one mode of operation data relative to activated keys in the console is transferred to the CPU and in another mode of operation data indicative of status is transferred from the CPU to the console.

5. From doc. 5, an arrangement is known comprising a central principal terminal combined with a CPU and a number of external auxiliary terminals (equivalent to operator consoles) each having a keyboard and in which data representing keyboard activation is transferred from each auxiliary to the principal terminal. Basically, the arrangement operates in the following manner: The central unit comprises a recirculating binary counter which is continually incremented, generating successively a number of codes (i.e. a count sequence of reference signals) representing all key positions (page 4, lines 23-37). These codes are transmitted to the auxiliary units and compared to the actual states of the keys. In case of correspondence a signal is provided on a single output line (page 3, line 27 - page 4, line 2). In the central unit this signal causes the counter to be stopped and its actually generated code to be read and transmitted to the CPU (page 6, line 24 - page 7, line 6) in the same manner as for the keyboard of the principal unit.

6. Doc. 5 relates clearly to the same field of art as the invention and the skilled person will readily appreciate that by the manner of transferring the states of keys to the CPU disclosed in doc. 5 effectively a data transfer (the reference signals produced by the counter) from the CPU to the console take place over the bus only when the counter is incrementing, which consequently will permit the transfer of other data (e.g. an acknowledging signal to

LED's in the console) in the same direction over the same bus conductors when no such reference signals are present, thereby saving a number of conductors and making efficient use of the input/output pins on a CPU chip. Applying the teaching from doc. 5 to the arrangement known from doc. 2, the skilled person would arrive at the subject-matter of Claim 1 without an inventive step being involved. Claim 1 must, therefore, be held unallowable.

7. The dependent claims 2-8 describe further embodiments of the arrangement according to Claim 1. These claims must share the fate of Claim 1 from which they depend. Apart from that, the Board has been unable to appreciate an inventive step in any of these claims as set out in the communication dated 23.02.89.

Order

For these reasons, it is decided that:

The appeal is dismissed.

The Registrar: **The Chairman:**

S. Fabiani P.K.J. van den Berg