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Bezeichnung der Erfindung: Logarithmic amplifiers
Title of invention:
Titre de l'invention :

Klassifikation / Classification / Classement : G 06 G 7/24

ENTSCHEIDUNG / DECISION
vom / of / du 15 June 1988

Anmelder / Applicant / Demandeur : United Kingdom Atomic Energy Authority

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Articles 56, 113(1), Rule 67

Schlagwort / Keyword / Mot clé : "Inventive step (yes)"- "Reimbursement of appeal fee (no)"

Leitsatz / Headnote / Sommaire

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Case Number : T 299/85 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 15 June 1988

Appellant : United Kingdom Atomic Energy Authority
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Representative : Collingwood A.R.
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Decision under appeal : Decision of Examining Division 066 of the European Patent Office given on 12 March 1985 and despatched on 25 July 1985 refusing European patent application No. 82 301 139.0 pursuant to Article 97(1) EPC

Composition of the Board :

Chairman : P. Ford
Members : W.B. Oettinger
Y. van Henden

Summary of Facts and Submissions

I. European patent application No. 82 301 139.0, filed on 5 March 1982 claiming a priority of 6 March 1981 and published under No. 60 662, was refused by a decision given in oral proceedings, held on 12 March 1985, by Examining Division 2.2.01.066.

The reason given for the refusal, stated in a written decision dated 25 July 1985, was that the subject-matter of Claim 1 filed on 12 March 1985 lacked an inventive step having regard to the prior art represented by the following documents:

(D1) Proceedings of the National Electronics Conference Volume 32, October 1978, pages 242 to 247

(D2) Nachrichten Technik - Elektronik, Volume 31 No. 2, 1981, pages 77 to 81

(D3) US-A-3 435 353

More particularly, the Examining Division held that the subject-matter of Claim 1 was obvious in view of Figure 3 of D1 and Figure 3 of D3, and that it was not relevant that other pieces of prior art showed other solutions to the problem addressed.

The more detailed embodiment shown in Figure 2 of the application was found not to go beyond normal practice of the person skilled in the art.

The following references, cited in the examination procedure either by the examiner or by the applicant, were not used in the decision:

(D4) IEEE Journal of Solid State Circuits, Volume SC-15 No. 3, June 1980, pages 291 to 295

(D5) Electronics, Volume 45 No. 3, January 1972, pages 70 to 72

(D6) Hewlett Packard Manual relating to 8808A log level preamplifier

(D7) Measurement Techniques, Volume 22 No. 8, August 1979, pages 975 to 976

II. On 16 September 1985, the Appellant lodged an appeal against this decision and paid the appeal fee.

In a statement of grounds of appeal, filed on 16 November 1985, the Appellant contested the Examining Division's finding.

Moreover he asserted a procedural violation in the Examining Division having introduced a technical point on which the decision under appeal relies, namely that there was a phasing problem which had a definite influence on the demodulated signal in D3, only after the decision had been announced at the conclusion of the oral proceedings. Reimbursement of the appeal fee was accordingly requested.

III. During the appeal procedure, the Board took the provisional view that, in effect, the refusal of Claim 1 on file was justified, but that a claim based on the embodiment disclosed in Figure 2 might appear acceptable.

IV. In response to this, the Appellant eventually, on 11 May 1988, filed such a claim.

This claim reads as follows:

"A logarithmic amplifier for handling a large dynamic range of high frequency a.c. input signals to produce an a.c. output signal which is a logarithmic function of the input signal, said logarithmic amplifier comprising a parallel cascade of a number of stages, each including an a.c. logarithmic converter and clipping means, input arrangements (R2, R4, R6) being connectable to a signal source which provides said a.c. input signal and being constructed so as to apply a different range of the input signal magnitude to each stage while maintaining a consistent phase of signal to each of the stages so that the input signal components each undergo the same degree of phase shifting as the other components and thereby leave said stages in phase with one another, and each stage being designed so as to clip the signal if it exceeds the logarithmic range of the respective stage, and a unit (4) for combining the a.c. outputs of all of said stages to derive a composite a.c. logarithmic output signal, characterised in that: the stage which handles the lowest range of input signal magnitude include an amplifier (5) amplifying the input signal component to that stage prior to conversion by the respective logarithmic converter (C1, R1, D1, D2, C2) and having a cut-off point in normal amplification operation; in that each of the higher stages also include an amplifier (6, 7) substantially identical to that in the lowest stage, all of said stage amplifiers (5, 6, 7) being in parallel with one another such that the input signal component handled by each stage undergoes normal amplification only by the amplifier of the respective stage and in that the logarithmic conversion is effected by a series arrangement of diodes (D17, D18; D21, D22) biased by a driver circuit (Q25, Q26, R54, R55, RV5, C27); and in that a network of anti-parallel diodes (D15, D16) is provided for reducing overshoot in the amplified

cut-off output of a corresponding amplifier whereby the corresponding diode log converter is provided, at the node common to the diodes of its series arrangement, with an output signal having an accurate cut-off point and the converted signal is taken from said node."

V. Subsequently, in a telephone conversation on 15 June 1988, the Appellant agreed to make consequential amendments in the description, noted below. It follows that the Appellant requests that the decision under appeal be set aside and a patent be granted on the basis of the following application documents:

Description: pages 1, 2 and 2a as filed on 25 June 1984 and with further amendments agreed on 15 June 1988,
pages 3 to 8 as published;
One claim filed on 11 May 1988;
Drawings, two sheets, as published.

In addition, the appellant maintains his request for reimbursement of the appeal fee.

An earlier request for oral proceedings has been withdrawn in view of the Board's positive attitude to the claim as now on file.

Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is, therefore, admissible.

2. The amendments made to the application meet the requirements of Article 123(2) EPC and are, therefore, admissible:

2.1 The claim is, generally, based on the original Claim 2 and, more specifically, restricted with respect of that original claim by such features of the embodiment described with reference to Figure 2 as can be regarded as being significant for the disclosed parallel cascade of log stages having separated amplifier and logarithmic functions and allowing a comparatively wide dynamic range to be achieved.

2.2 The amendments made to the description on 25 June 1984 together with those made at the request of the Board on 15 June 1988 are consistent with the amendemnts to the claim and with the scope of the application as originally filed.

3. No question of lack of novelty arises. Furthermore, the subject-matter of the claim involves an inventive step, for the following reasons:

3.1 In the art of logarithmic amplifiers it is usual to cascade several logarithmic stages.

Basically two different kinds of cascades can be distinguished: a parallel cascade and a serial cascade. The former is represented in D1 Figure 3 and in D3 Figure 3, the latter in D2 Figure 9, in D3 Figure 1, in D4 Figure 2, in D5 Figure 1 and in D6 Figure 4-1. A mixture of both is possible; such a case is represented in D1 Figure 4.

3.2 Depending on the intended application, speed of response is normally a requirement for logarithmic amplifiers, in particular if a signal is an a.c. signal.

In this respect it is well recognised that a parallel cascade is superior to a serial cascade, due to the fact that in a parallel cascade the inputs to all stages have no

phase differences whereas in a serial cascade each series amplifier (1 to N in Figure 1 of D5) introduces a small delay. This latter fact being the reason for proposals to compensate such delays (eg. by "delay" in Figure 1 of D5), it is clear that such proposals are irrevelant in cases in which there are inherently no delays, as in a parallel cascade.

3.3 The claimed invention makes use of a parallel cascade and thus of its inherent superiority in response speed.

For this reason, the prior art coming nearest to the claimed invention is considered to be D1, in particular Figure 3 and related parts of that document.

3.4 As a further requirement for logarithmic amplifiers, these must provide for a certain dynamic range of input signals.

In this respect, D1 discloses that its Figure 3 arrangement is limited to 15dB per stage and to a maximum number of three stages.

This limitation is the result of using the kind of log stages proposed in D1.

From the text on page 242 and from Figure 7 and the text relating to it, it can be derived that each log stage amplifies the signal in the signal range below its "active" range, whence it follows that it is an amplifier also at least in the lower part of its "active" range, but that otherwise the differential pairs of transistors used have a logarithmic output current versus input voltage characteristic (cf. Figure 2), whence it follows that signal amplification does not necessarily take place in the upper part of the "active" range, depending, as the skilled person knows, on the impedance of the output circuit.

3.5 As a solution to this dynamic range problem, D1 proposes the Figure 4 arrangement but the skilled person will immediately see that this arrangement is no more a pure parallel cascade and its speed of response will therefore be degraded somewhat unless the delay introduced by the amplifier (A) is compensated, as suggested by D5 Figure 1.

3.6 For this reason, the skilled person may be expected to look for other solutions of the dynamic range problem.

Being aware of the obvious relation of the limitations of the Figure 3 arrangement to the kind of log stages used (cf. 3.4) he will consider avoiding the combination of amplifying and logarithmic conversion functions in these stages.

A model for doing so is known to him in the form of the Figure 3 arrangement of D3, this arrangement using separate amplifying and logarithmic converting means in each log stage. Obviously by this separation each function can, independent of the other, be optimised and for this reasons, the skilled person can be expected to consider using a separate amplifier and logarithmic converter in each stage, knowing also that this does not degrade in any way the inherent speed of response advantage of the parallel cascade.

3.7 He will clearly not be deterred from such consideration by the mere fact that D3 relates to logarithmic amplifiers converting a.c. into d.c. which therefore have detectors in their log stages. It will be very clear to him from his general knowledge that, for achieving an a.c. output, he would only have to omit these detectors.

3.8 The invention as now claimed goes however beyond such considerations.

3.9 First, it proposes to use, as logarithmic converter, a series arrangement of diodes biased by a driver circuit, whereby the signal is fed to, and taken from, the node common to the diodes.

As regards this feature, the following is noted:

No diode arrangement is used in D1.

D3 discloses, as an example of a logarithmic converter, a parallel arrangement of differently biased diodes; no incentive to modify this arrangement can be derived from D3.

The serial diode arrangement used in the amplifier stage shown in Figure 13 of D2 has quite a different function. It serves only to switch, at a particular input signal level, the amplification of the respective stage to 0dB. The logarithmic conversion is not effected by these switches but by the combined characteristic of several stages.

Nothing relevant can be derived from D4, D5 or D6.

D7 shows a logarithmic amplifier comprising, in parallel cascade, a first log stage with an amplifier and a logarithmic converter and a second log stage consisting only of a logarithmic converter. In these logarithmic converters, use is made of an anti-parallel diode arrangement biased by a stabilised current to exhibit a logarithmic volt-ampère characteristic.

It may be the fact that a serial diode logarithmic converter as claimed is, in effect, equivalent to that anti-parallel diode arrangement, but there is no disclosure

of this equivalence in the prior art citations and, even if there were any, the claimed invention comprises more than the replacement of one arrangement by an equivalent.

3.10 As a further feature, the claimed invention employs an anti-parallel diode arrangement reducing overshoot in the amplifier cut-off output.

As to this feature the following is noted:

The only citation disclosing an anti-parallel diode arrangement is D7. However, that arrangement is biased so as to have a logarithmic function. No incentive to use such an arrangement for the quite different purpose of reducing overshoot can thus be derived from D7.

Furthermore, even on the assumption, previously made in a communication by the Board and not challenged by the Appellant, that anti-parallel diode arrangements for reducing overshoot are general knowledge per se, it does not necessarily follow that the particular arrangement now claimed in combination is obvious.

3.11 The claimed invention must be seen as a whole.

Putting its various pieces together and comparing that combination with the prior art, the invention presents itself in the following way:

Starting from a parallel cascade of log stages (D1 Figure 3):

(a) Instead of differential amplifiers (Figure 2 and 7) as log stages, separated amplifiers and logarithmic converters (as in D3 Figure 3) are used;

(b) The amplifiers are supplemented by anti-parallel diodes reducing overshoot;

(c) Instead of anti-parallel diodes (as in D7) or any other kind of circuit as logarithmic converters, a properly biased serial diode arrangement is used (only known per se from D2 in a function which is not comparable to the one used here).

3.12 Whether or not it is obvious to apply one or two of these features in a logarithmic amplifier of the kind in question, it is only relevant to the present case whether it is obvious to combine all three.

In deciding on this point, also the results of this combination must be considered.

In this respect, the following is noted:

It has been submitted that the embodiment shown in Figure 2 allows a dynamic range of 35dB per stage to be achieved. The Board has no reason to doubt the correctness of this submission. Further, the Board is satisfied that this quantatitive result is the result of the essential technical features of that embodiment which consists in (a) the use of separate amplifiers, (b) reducing any overshoot in their output, (c) the use of a properly biased series diode arrangement as logarithmic converter.

In contrast, D1 discloses the achievement of only 15dB per stage and no higher values are disclosed in any other prior art citation (including D4 and D5).

An improvement by 20dB must be regarded as outstanding and unexpected, even if some improvement could be expected from the application of feature (a) alone (cf. paragraph 3.6).

It is therefore to be taken as an indication that the claimed combination of features does involve an inventive step.

4. In accordance with Rule 67 EPC, reimbursement of an appeal fee shall be ordered when a Board of Appeal deems an appeal to be allowable "if such reimbursement is equitable by reason of a substantial procedural violation." In the present case, the Appellant asserts that there was such a violation (in contravention of Article 113(1) EPC) in that, both when announcing its decision at the end of oral proceedings and in the written reasons for decision, the Examining Division made and relied upon the assertion that phase difference generated in the a.c. amplifiers of D3 would have an effect on the d.c. output signal. In the written reasons for decision this was stated to be "self evident". Nothing in the file of the case shows that this point was ever raised in writing or orally with the Appellant prior to the announcement of the decision. Prima facie, therefore, this was an assertion of technical fact which should have been discussed with the Appellant (who disputes it) before the decision was announced and the Examining Division's failure to do so amounted to a breach of the requirements of Article 113(1) EPC. However, this does not seem to have been a major point in the decision under appeal and is not a point on which the present appeal is being allowed. Indeed, without the substantial amendments in the main claim now made, the appeal could not have been allowed. In these circumstances, the Board is unable to conclude that reimbursement would be equitable by reason of a substantial procedural violation. Accordingly, reimbursement of the appeal fee cannot be ordered.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent on the basis of the following application documents:

   (a) Claim filed on 11 May 1988;

   (b) description pages 1, 2 and 2a filed on 25 June 1984 with the provision that

      (i) the text from line 16 on page 2 up to and including line 5 on page 2a is replaced by the wording of the Claim but without reference numerals, and

      (ii) the sentence bridging lines 6 and 7 on page 2a is deleted;

   (c) description pages 3 to 8 as published;

   (d) drawings, two sheets, as published.

3. The request for reimbursement of the appeal fee is rejected.

The Registrar: The Chairman:

S. Fabiani P. Ford