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Bezeichnung der Erfindung: Integrated circuit information processor
Title of invention:
Titre de l'invention :

Klassifikation / Classification / Classement : G 06 F 5/00

ENTSCHEIDUNG / DECISION

vom / of / du 9 December 1987

Anmelder / Applicant / Demandeur : K.K. Toshiba

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Art. 56

Kennwort / Keyword / Mot clé : "Inventive step (no)"

Leitsatz / Headnote / Sommaire

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Case Number : T 20/86

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 9 December 1987

Appellant : KABUSHIKI KAISHA TOSHIBA
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Decision under appeal : Decision of Examining Division 065 of the European Patent Office dated 7 May 1985* refusing European patent application No. 82 301 894.0 pursuant to Article 97(1) EPC

* posted on 23 August 1985

Composition of the Board :

Chairman : P.K.J. van den Berg
Members : W.B. Oettinger
F. Benussi

Summary of Facts and Submissions

I. European patent application No. 82 301 894.0 filed on 8 April 1982 claiming a priority of 21 May 1981 and published under No. 66 360 was refused by a decision of Examining Division 2.2.01.065 dispatched on 23 August 1985.

II. The reason given for the refusal was that the subject-matter of Claims 1 to 6 filed on 27 June 1984 lacked an inventive step in view of the prior art, in particular GB-A-1 143 360 (D4), and that the same applied to Claims 1 to 6 filed on 16 April 1985 as an auxiliary request.

In respect of a technological feature in Claim 5 of the main request, and in Claim 2 of the auxiliary request, relating to the burying of transfer gates beneath data bus lines, the Examining Division referred to the well-known planar technology for integrated circuit production.

III. On 23 October 1985 the applicant gave notice of appeal against that decision, having paid the appropriate fee on 22 October 1985.

IV. In a statement of grounds of appeal, filed on 23 December 1985, the Appellant essentially argued that D4 does, in particular, not disclose the above-mentioned technological feature of the invention.

A new set of Claims 1-5 with Claim 1 having this feature accompanied that statement.

V. In a communication of the Board, dated 19 August 1987, the Rapporteur raised the objection that the amendments made to Claim 1, and also those made to Claim 5, would introduce matter which extends beyond the content of the application

as filed and are, therefore, inadmissible under Article 123(2) EPC.

Further, the Rapporteur documented the prior art, as regards the planar technology, by citing IEEE Spectrum, October 1969, pages 28-35 (D5).

In respect of the inventive step issue, he expressed the provisional opinion that it is obvious to implement the AND gates 413 in the rotation control gates 9 (RCG0 to RCG29) of the device in Fig. 15a of D4 in a way as is proposed in D5 for gates in logic circuits generally, and that such an implementation would be a device as claimed, including the feature of burying the transfer gates between the data bus lines.

VI. On the request of the Appellant, oral proceedings were held on 9 December 1987. In these, the Appellant re-amended Claim 1 filed on 23 December 1985 by replacing the word "beneath" (in line 15) by the expression "below and between", so as to meet the objection made under Article 123(2) EPC. Claim 1 then reads as follows:

"1. An integrated circuit information processing device having an input data bus (1) electrically incorporated into said device including input lines, an output data bus (L) electrically incorporated in said device including output lines, and transfer means, electrically connected between said input bus and output bus, characterized in that said transfer means comprises a plurality of transfer gates arranged in a single stage, each of which is connected between a specific line of said input bus and a specific line of said output bus in such a way that said transfer gates form a desired bit pattern, in that said information processing device further comprises means for simultaneously driving said transfer gates, and in that

said transfer gates are buried below and between said input data bus and said output data bus".

Dependent Claims 2 to 5 concern particular embodiments of this device performing particular kinds of bit manipulation.

In respect of Claim 5 the Appellant declared his willingness to an amendment as considered necessary by the Board to meet the objection made.

The Appellant requests that the decision under appeal be set aside and a patent be granted on the basis of Claims 1-5 so amended. This request is considered to imply the inclusion of a correspondingly amended description and of the drawings on file.

VII. In respect of the question of inventive step at issue, the Appellant argues essentially as follows:

A first feature distinguishing the claimed invention from the D4 device is that the transfer gates constitute a single stage while the source selection gates 3 and rotation control gates 9 of D4 together form two stage gates.
A further, important, distinguishing feature is that the transfer gates are buried below and between the data bus lines. The FET of Fig. 3B and C of D5 is practically in alignment with the metal interconnections and these latter are not bus lines.

Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is, therefore, admissible.

2. The application documents as on file are considered to meet the requirements of Article 123(2) EPC, as follows:

2.1 Claim 1 adds, to the original Claim 1, only such features as are disclosed in the description.

The last feature of this claim is based on page 7 lines 6-8. From the expression "buried" it can be derived that the transfer gates are located in a certain depth below the bus lines; and although the expression "between the bus line" is formally unclear it cannot, in the context (p.7, lines 3-6) reasonably be interpreted in any other way than as meaning "between the bus lines" or, more precisely, "between (the lines of) the input data bus and (the lines of) the output data bus".

2.2 From the fact that Claim 5 is a dependent claim referring back to Claim 1, and from the further fact that Claim 5 is clearly intended to cover the embodiment shown in Fig. 4 and described with reference to Fig. 2, it follows that Claim 1 must be read without its (formal) restriction to a "plurality" of transfer gates being buried below and between the input and output data busses.

This, however, causes no objection under Art. 123(2) EPC. In both its literal (a "plurality" of transfer gates) and its broad (one or more transfer gates) interpretation, the subject-matter of this claim is disclosed in the description.

2.3 No problem arises either from the inadmissibility of Claim 5 in its present form. The Appellant declared that this claim should be re-amended so as to meet the objection made under Article 123(2) EPC. The Board considers that this means that Claim 5 would, in substance, correspond to the original Claim 4 when appended to Claim 3.

2.4 The other dependent claims are supported by the description referring to Fig. 1, Fig. 5A and Fig. 5B, respectively.

3. While the subject-matter of Claim 1 in either interpretation (cf. para. 2.2 above) is clearly novel (Art. 54), it does not involve an inventive step (Art. 56) and is, therefore, not patentable (Art. 52(1) EPC).

These conclusions are based on the following facts and considerations:

3.1 With regard in particular to the present form of Claim 1, D4 represents the prior art coming nearest to the claimed invention.

Whether this is still true when the interpretation of Claim 1 covering the embodiment shown in Fig. 4 and described with reference to Fig. 2 is taken into account (cf. para. 2.2 above) needs not to be decided.

In any case, D4, in particular Fig. 15a, discloses a device according to the precharacterising portion of Claim 1. It consists in one of the four gates (e.g. the one denominated 415) in the first one (RCG0) of the rotation control gates 9 and of all corresponding other gates in rotation control gates RCG1 through RCG29. The input lines to these gates are considered to constitute an input data bus, the output lines (denominated e.g. 15, 16, 14) an output data bus, and the gates (415) a transfer means as defined in Claim 1.

3.2 This known device has the characterising feature of Claim 1 that the transfer means comprises a plurality of transfer gates (e.g. 415) arranged in a single stage. Each of these gates is connected between a specific line of the input bus

and a specific line (e.g. 15, 16, 14) of the output bus so as to form a desired bit pattern, namely one which is shifted, or rotated, left by a certain number, e.g. 15, of bits with respect to the input bit pattern (page 15, lines 103-107).

No reason is seen why the source selection gates 3 (SSG0 through SSG29), or the transfer logic control gates 11 (TCG0 through TCG29) should be considered as constituting a part of the rotation control gates 9. The Board does not therefore agree with the Appellant's opinion that the transfer gates in the known device are arranged in two stages.

3.3 The known device has, furthermore, the characterising feature of Claim 1 in that it comprises means (indicated e.g. by $\overline{R3}$) for simultaneously driving said transfer gates (cf. page 15, lines 80-82 and 103-104).

3.4 No particular implementation is proposed in D4 for the rotation control gates 9 (e.g 415). It is only indicated, by the use of a corresponding symbol in Fig. 15a, that these gates perform an AND function.

The skilled person is therefore free to choose any known means suitable for this purpose.

3.5 The Appellant submits that the usual implementation of AND gates requires power lines and earth lines and that the skilled person would therefore implement the rotation control gates 9 of D4 likewise. In this case, it is submitted, it would be difficult, if not impossible, to bury the transfer gates below and between the input and output bus lines.

3.6 However, it is to be noted that nothing in D4 points to this kind of implementation as the only possible one.

3.7 D5 discloses another kind of implementation for gates performing a logic AND function (cf. page 28 right-hand column No. 1 and 2).

As regards this function these gates must therefore be considered as being equivalent to those mentioned above (3.5) and their use as obvious to the person skilled in the art.

3.8 The gates of D5 consist of field-effect transistors (page 28 left-hand column, first paragraph) and can be combined in integrated circuits (first and second paragraph).

Fig. 3 shows the structure of such FETs made according to the process described in D5. The active region of the transistor (as indicated by Si_3N_4 and SiO_2) is buried within a layer of silicon dioxide partly covered by metal (aluminium) layers (Fig. 3B) serving as source and drain contact lines (Fig. 3C) and forming the desired interconnection patterns (page 30 left-hand column, third paragraph).

Thus, a gate made according to D5 would be buried below the interconnection lines of the integrated circuit. Further, if source and drain of the FET are used, as is conventional, as the input and output of the FET, such a gate would lie between the input and output lines of the interconnections pattern.

3.9 Consequently, if as is obvious (3.7), gates of the D5 type are used in the D4 device, these gates would be buried

below and between the metal interconnection lines which serve as input and output lines of the data busses.

It is true that those parts of the metal layer which contact the source and drain electrodes do not lie above the FET. However, as became clear in the oral proceedings, also in the claimed device some kind of lead must be provided for connecting the input and output electrodes of the transfer gates with the input and output data bus lines lying at a higher level of the i.c. substrate.

In the absence of any disclosed details, it can reasonably be assumed that these connections can have the same form as in D5.

3.10 As a consequence, the last characterising feature in Claim 1 would be fulfilled if the D4 device having all other features of that claim is implemented in a way as suggested by D5. The subject-matter of Claim 1 is therefore considered to be obvious having regard to this state of the art.

3.11 While this applies in particular to Claim 1 when taken literally (embodiments of Fig. 3 and 6) no other conclusion could be drawn for the even simpler case that according to a more general interpretation of Claim 1 (of para. 2.2 above), only a single transfer gate is present (embodiment according to Fig. 4) and implemented according to the last characterising feature in Claim 1.

4. Claim 1 falling for these reasons, also the dependent Claims 2 to 5 are not allowable.

Moreover, no independent claim based on any of these claims has been presented and no arguments have been advanced

which could support a more favourable view on the subject-matter of any of them.

Order

For these reasons, it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

S. Fabiani Mr van den Berg