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Veröffentlichung im Amtsblatt	~~Ja~~/Nein
Publication in the Official Journal	~~Yes~~/No
Publication au Journal Officiel	~~Oui~~/Non

001328

Aktenzeichen / Case Number / N° du recours : T 94/86 - 3.5.1

Anmeldenummer / Filing No / N° de la demande : 81 108 170.2

Veröffentlichungs-Nr. / Publication No / N° de la publication : 50 772

Bezeichnung der Erfindung:
Title of invention:
Titre de l'invention : JFET dynamic memory

Klassifikation / Classification / Classement : G11C 11/24, H01L 27/10

ENTSCHEIDUNG / DECISION
vom / of / du 25 January 1989

Anmelder / Applicant / Demandeur : Burroughs Corporation
(a Delaware Corporation)

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Article 56

Schlagwort / Keyword / Mot clé : "Inventive step (no)"

Leitsatz / Headnote / Sommaire

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Case Number : T 94/86 - 3.5.1

DECISION
of the Technical Board of Appeal 3.5.1
of 25 January 1989

Appellant :
Burroughs Corporation (a Delaware Corporation)
Burroughs Place
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Representative :
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Decision under appeal : Decision of Examining Division 067 of the European Patent Office dated 7 November 1985 refusing European patent application No. 81 108 170.2 pursuant to Article 97(1) EPC

Composition of the Board :

Chairman : P.K.J. van den Berg
Members : W.J.L. Wheeler
E. Persson

Summary of Facts and Submissions

I. European patent application No. 81 108 170.2, filed on 10 October 1981, claiming priority of 27 October 1980 from a previous application in the United States of America (US 200997), was refused by a decision of the Examining Division 067 of the European Patent Office dated 7 November 1985. That decision was based on Claims 1 to 4 filed with a letter dated 26 July 1985.

II. The reason given for that decision was that the subject-matter of Claim 1 did not involve an inventive step, having regard to the prior art known from the following documents:

(1) GB-A-2 011 175
(2) US-A-3 387 286
(3) Rudolf Müller: Bauelemente der Halbleiter-Elektronik, 1979, pages 130 to 136
(4) US-A-3 740 731.

III. On 8 January 1986, the Appellant filed a notice of appeal against that decision. The fee for appeal was paid on the same day. A statement of grounds was filed on 8 March 1986, accompanied by a new set of claims 1 to 4 (main petition) and a second set of claims 1 and 2 (auxiliary petition).

IV. In a communication pursuant to Article 11(2) of the Rules of Procedure of the Boards of Appeal, the provisional opinion was expressed that a person skilled in the art, starting from D1 and applying his own common general knowledge in the art in order to optimise the design, would arrive at a dynamic memory device falling within the scope of Claim 1 of the main petition, without having to exercise any inventive skill. As evidence for the general knowledge in the art, the following document was cited:

(D5) The New Penguin Dictionary of Electronics, 1979, pages 167 to 172.

V. Oral proceedings took place on 25 January 1989, at which the Appellant requested that the decision under appeal be set aside and a patent granted on the basis of Claims 1 to 4 (main petition), subject to the deletion of the words "non-punchthrough type of" in line 2 of Claim 1 (main request); or on the basis of the claims specified in the main request, with the insertion of the words ''and said storage capacitor (12) consisting of a reverse biased P-N-junction, and" after the word "drain," in line 8 of Claim 1 (first auxiliary request); or on the basis of Claims 1 and 2 (auxiliary petition), subject to the deletion of the words "non-punchthrough type of" in line 2 of Claim 1 (second auxiliary request).

VI. Claim 1 of the main request is worded as follows:

"1. A dynamic memory device comprising a plurality of dynamic memory cells (10) each having a junction field-effect transistor (11) having a source, a gate, a drain and a negative threshold voltage V_T and a capacitor (12) coupled to said drain for storing voltages representing information received therefrom, whereby each transistor's gate is reverse biased with respect to its source and drain, said memory device further comprising a plurality of word lines WL and a plurality of bit lines BL, each of said word lines WL being coupled directly both to the gates of respective rows of said transistors (11) and to a memory cell selection means (20) for applying a voltage V_{GH} directly on said gate to select said dynamic memory cell, and for applying a voltage V_{GL} directly on said gate to deselect said dynamic memory cell, and each of said bit lines BL being coupled to the source of respective columns of said transistors (11) and to a column select transistor (31), said column select transistors (31) being coupled to a memory cell write means (30) which for writing information into a selected dynamic memory cell (10) applies a voltage V_H on said source to write a high voltage in said capacitor (12) where $V_{GH} - V_T > V_H$, and which applies a voltage V_L on said source to write a low voltage in said capacitor (12) where $V_{GL} - V_T < V_L$ and $V_L > V_{GH}$ and whereby for reading information from a particular memory cell said memory cell selection means (20) initially applies said voltage V_{GL} to all of said word lines WL, thereinafter said memory cell write means applies said voltage V_H to all of the bit lines BL for precharging them to said voltage V_H and thereinafter both said memory cell write means (30) and said column select transistors (31) are turned off and said memory cell selection means (20) applies said voltage V_{GH} to that word line WL which is coupled to said dynamic memory cell (10) that is to be read and the bit lines BL are sensed by sense amplifiers SA to detect whether the bit line voltage of the bit line BL coupled to said dynamic memory cell to be sensed drops from its precharged value to some lower value or remains on the bit line BL depending upon whether or not said voltage V_L was stored in the selected dynamic memory cell (10), said dynamic memory cells (10), said memory cell selection means (20), said memory cell write means (30) and said column select transistors (31) being all integrated on a single semi-conductor substrate (50)."

Claims 2 to 4 of the main request are dependent upon Claim 1.

Claim 1 of the second auxiliary request is worded as follows:

"1. A dynamic memory device comprising a plurality of dynamic memory cells (10) each having a junction field-effect transistor (11) having a source, a gate, a drain and a negative threshold voltage V_T and a capacitor (12) coupled to said drain for storing voltages representing information received therefrom, whereby each transistor's gate is reverse biased with respect to its source and drain, said memory device further comprising a plurality of word lines WL and a plurality of bit lines BL, said dynamic memory cells (10) being arranged on a semiconductor substrate (50) of a P-type, said semiconductor substrate (50) having a patterned field oxide layer (51) defining the perimeters of each of said dynamic memory cells (10), each dynamic memory cell (10) having

a) a P-N-junction (60) as said storage capacitor (12) by implanting P-type dopant atoms into a region (61) and forming an N^+ semiconductor layer (62a, 62b) over this structure,

b) said N^+ semiconductor layer (62a, 62b) being patterned to form two polycrystalline regions one of which regions (62a) is isolated from other dynamic memory cells (10) whereas the other region (62b) forms said bit line BL which interconnects several dynamic memory cells (10),

c) an N^- channel region (63) by implanting dopant atoms into that portion of said semiconductor substrate (50) which lies between the polycrystalline regions (62a, 62b) for forming the drain of said transistor (11),

d) N-type regions (64a, 64b) below said polycrystalline region (62a, 62b) one of said N-type regions (64a) forming the source of said transistor (11) whereas the other region (64b) combines with said implanted region (61) to form said P-N-junction (60),

e) a patterned insulating layer (65, 73) being formed over said structure which patterned insulating layer (65, 73) has an opening over said channel region (63), and

f) a metal gate (66) which is fabricated in the opening over said channel region (63) to form a Schottky junction with said channel region (63), said metal gate (66, 74) being the gate of said transistor (11),

each of said word lines WL being coupled directly both to the gates of respective rows of said transistors (11) and to a memory cell selection means (20) for applying a voltage V_{GH} directly on said gate to select said dynamic memory cell, and for applying a voltage V_{GL} directly on said gate to deselect said dynamic memory cell, and each of said bit lines BL being coupled to the source of respective columns of said transistors (11) and to a column select transistor (31), said column select transistors (31) being coupled to a memory cell write means (30) which for writing information into a selected dynamic memory cell (10) applies a voltage V_H on said source to write a high voltage in said capacitor (12) where $V_{GH} - V_T > V_H$, and which applies a voltage V_L on said source to write a low voltage in said capacitor (12) where $V_{GL} - V_T < V_L$ and $V_L > V_{GH}$ and whereby for reading information from a particular memory cell said memory cell selection means (20) initially applies said voltage V_{GL} to all of said word lines WL, thereinafter said memory cell write means applies said voltage V_H to all of the bit lines BL for precharging them to said voltage V_H and thereinafter both said memory cell write means (30) and said column select transistors (31) are turned off and said memory cell selection means (20) applies said voltage V_{GH} to that word line WL which is coupled to said dynamic memory cell (10) that is to be read and the bit lines BL are sensed by sense amplifiers SA to detect whether the bit line voltage of the bit line BL coupled to said dynamic memory cell to be sensed drops from its precharged value to some lower value or remains on the bit line BL depending upon whether or not said voltage V_L was stored in the selected dynamic memory cell (10), said dynamic memory cells (10), said memory cell selection means (20), said memory cell write means (30) and said column select transistors (31) being all integrated on a single semiconductor substrate (50)."

Claim 2 of the second auxiliary request is dependent upon Claim 1.

VII. The Appellant argued in effect that GB-A-2 011 175 (D1) was mainly concerned with the provision of charge storage regions (28, figure 2) of large storage capacity. Most of the embodiments used IGFETs, which, according to the Appellant, were generally preferred to JFETs, because JFETs required a permanently reverse biased gate, and therefore more complicated circuitry. Although figure 5 showed a JFET, there was no express disclosure in D1 that this JFET had a negative threshold or that its gate was reverse biased. D1 did not expressly describe any memory cell selection means, nor did it describe column select transistors coupled to memory cell write means. D1 gave no indication of the voltage requirements for the word lines and bit lines, nor did it disclose a method of read out including the preliminary steps of applying a certain voltage to all the word lines and then precharging all the bit lines to a predetermined voltage. Finally, D1 did not disclose memory cell selection means, column select transistors and memory cell write means integrated on the same semiconductor substrate as the memory cells.

The invention overcame a prejudice against JFETs and was based on recognising that the insulation layer under the gate of an IGFET was not always sufficiently reliable and that a JFET could afford better insulation, if the gate was reverse biased and the operating voltages were correctly chosen. The operating voltages (see figure 2 of the present application) were different from those used with IGFETs. Several steps would be needed to get from D1 to the invention.

Regarding the auxiliary requests, the Appellant pointed out that D1 did not disclose a P-N-junction capacitor. The combination of JFET and P-N-junction capacitor was advantageous, because it made it possible to simplify the manufacturing process. Although D4 described a P-N-junction capacitor it did not mention JFETs.

Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is, therefore, admissible.

2. Novelty

The Board agrees with the Appellant that the closest prior art cited, namely GB-A-2 011 175 (D1), does not disclose all the features specified in the independent claims of the main and auxiliary requests. The dynamic memory devices as claimed in these claims are therefore new.

3. Inventive step (main request)

3.1 D1 explicitly discloses a dynamic memory device comprising the following features in common with Claim 1 of the main request:

a plurality of dynamic memory cells (12) arranged in rows and columns, wherein, in the embodiment shown in figure 5 and in one of the alternatives described with reference to figure 6, each memory cell consists of a JFET and a capacitor for storing voltages representing information (see D1, figures 1, 5 and 6, page 1, lines 70 to 107, page 2, lines 34 to 49, and page 4, lines 59 to 109);

a plurality of word lines (14), each word line being coupled directly to the gates of the FETs of the cells in a respective row, and means for applying a voltage directly on said gates to select and deselect the memory cells in the row (see D1, page 1, lines 92 to 100 and 108 to 129, and page 3, lines 29 to 39 and 57 to 67);

a plurality of bit lines (16), each bit line being coupled to the sources of the FETs of the cells in a respective column, and means for applying a voltage on said sources representing information to be written into a selected memory cell (see D1, page 1, lines 108 to 117, page 3, lines 29 to 42);

in which, for read out of the information stored in a particular cell, the bit line is brought to a predetermined potential, the select voltage is then applied to the word line and the bit line is sensed by a sense amplifier (see D1, page 3, lines 57 to 74).

3.2 However, in the opinion of the Board, a person skilled in the art would derive more from D1 than its explicit disclosure. A person skilled in the art, reading D1 in the light of his own general knowledge, would know that an N-channel JFET (see D1, figure 5 and page 4, lines 59 to 74) always has a negative threshold voltage and that it is necessary to maintain its gate reverse biased with respect to its source and drain at all times (see D5, pages 167 to 172, in particular, page 171, lines 4 to 9 and figure k, and page 172, lines 19 to 24). Thus, to a skilled reader, the explicit disclosure of an N-channel JFET in D1 is tantamount to saying an N-channel JFET having a source and a drain, a negative threshold voltage and a gate reverse biased with respect to its source and drain.

Furthermore, in the light of the explanation given in D1 at page 1, line 70 to page 2, line 5, the skilled reader would realise that the described operations for writing in and reading out applied to all the embodiments. It would also be clear to him from page 3, lines 75 to 81, particularly in view of the reference there to conservation of charge, that during sensing by the sense amplifier the bit lines must be isolated from the means for applying the voltages representing information to be written in.

3.3 The dynamic memory device claimed in Claim 1 of the main request therefore differs from the teaching which a person skilled in the art would derive from D1 in that:

(a) column select transistors are provided, which are coupled to respective bit lines and to a memory cell write means;

(b) the memory cell write means applies a voltage V_H, on the appropriate bit line to write a high voltage in the capacitor where $V_{GH} - V_T$ is greater than V_H, and applies a voltage V_L on the appropriate bit line to write a low voltage in the capacitor where $V_{GL} - V_T$ is less than V_L and V_L is greater than V_{GH};

(c) for reading out, the memory cell selection means initially applies the deselect voltage V_{GL} to all the word lines and thereafter the memory cell write means applies the voltage V_H to all the bit lines for pre-charging them to V_H, with the consequence that during the sensing step proper the sense amplifiers detect whether or not the voltages on the bit lines drop from the precharged value; and

(d) the memory cells, selection means, write means and column select transistors are all integrated on a single semiconductor substrate.

3.4 The objective problem solved by the claimed device is therefore not the one of overcoming the disadvantages of IGFETs mentioned in the present application at page 1, line 22 to page 2, line 16, but rather that of filling in certain practical details not explicitly described in D1. In the opinion of the Board, this is an obvious problem to want to solve.

3.5 A person skilled in the art would deduce from D1, page 3, lines 29 to 32 and 57 to 64, that some sort of switching means must be provided for selecting bit lines (columns) for writing, and from his practical knowledge he would know that transistors (which may therefore be called column select transistors in the terminology used in Claim 1) would be suitable. The Board notes that the claim does not specify the precise disposition of the column select transistors, but merely stipulates in a very general way that each bit line is coupled to a column select transistor, said column select transistors being coupled to a memory cell write means. In the opinion of the Board, any practical arrangement would necessarily satisfy this very general requirement.

A person skilled in the art would realise that in order to guarantee the required permanent reverse bias of the gates of the JFETs, the lowest voltage applied to the source (V_L) must be higher than the highest voltage applied to the gate (V_{GH}). He would also realise that in order to be able to transfer the high voltage (V_H) on a bit line onto the capacitor of a memory cell, the row selecting voltage on the gate (V_{GH}) must be higher than the sum of the voltage on the source (V_H) and the threshold voltage (V_T). He would also realise that in order to be able to deselect a cell, the deselect voltage on the gate (V_{GL}) must be lower than the sum of the lower voltage on the source (V_L) and the threshold voltage (V_T). In other words, he would choose values of V_T, V_{GH}, V_{GL}, V_H and V_L meeting the conditions specified for them in Claim 1.

It would also be clear to a person skilled in the art that for reading out it is necessary as a preliminary step to apply the deselect voltage V_{GL} to the gates of all the memory cells to preserve the stored information before forcing the bit lines to a predetermined state. Although the precharging of the bit lines to V_H does not appear to be absolutely necessary, since, even if the bit lines were at V_L when the word line was raised to V_{GH}, the gates would still remain reverse biased (the voltage on the bit line would rise if the capacitor of a cell being read stored V_H, or would remain at V_L if this capacitor stored V_L), it would nevertheless be obvious to a person skilled in the art that out of the two available predetermined states (V_L and V_H) to which the bit lines could be forced, the higher one (V_H) is the one which affords the greater safety margin.

Finally, in the absence of any reason to do otherwise, a person skilled in the art would automatically follow the conventional practice of integrating the memory cells, selection means and write means (including column select transistors) on a single semiconductor substrate (otherwise more than 250 pins would be needed for a 64k memory).

3.6 In the opinion of the Board, a person skilled in the art, starting from D1 and applying his own common general knowledge in the art (as evidenced by D5) in order to devise a practical embodiment, would arrive at a dynamic memory device falling within the scope of Claim 1 of the main request, without having to exercise any inventive skill. The Board therefore considers that the subject-matter of Claim 1 of the main request does not involve an inventive step within the meaning of Article 56 EPC and consequently does not meet the requirements of Article 52(1) EPC.

3.7 It follows that the main request cannot be allowed.

4. Inventive step (first auxiliary request)

4.1 The memory device according to Claim 1 of the first auxiliary request differs from that according to Claim 1 of the main request only in that the capacitor (12) is in the form of a reverse biased P-N-junction. It is common general knowledge in the art that a reverse biased P-N-junction can be used as a capacitor. US-A-3 740 731 (D4) discloses a DRAM wherein the memory cells consist of an IGFET and a P-N-junction, which a person skilled in the art would know must be reverse biased to prevent the charge being conducted away.

4.2 In the opinion of the Board, it is obvious to provide a dynamic memory device in which the memory cells each comprise a JFET (known from D1) whose drain is connected to a capacitor in the form of a P-N-junction (known from D4). For the reasons given under 3.5 and 3.6 above, the resulting dynamic memory device would be in accordance with Claim 1 of the first auxiliary request. The Board therefore considers that the subject-matter of Claim 1 of the first auxiliary request does not involve an inventive step within the meaning of Article 56 EPC and consequently does not meet the requirements of Article 52(1) EPC.

4.3 It follows that the first auxiliary request cannot be allowed.

5. Inventive step (second auxiliary request)

5.1 Claim 1 of the second auxiliary request differs from Claim 1 of the main request in that details of the various layers and regions on the semiconductor substrate have been included.

5.2 D4 discloses a dynamic memory device comprising many of the features of Claim 1 of the second auxiliary request. The dynamic memory device disclosed in D4 comprises:

a plurality of dynamic memory cells (10, see figures 1 and 2) arranged in rows and columns, each memory cell having an IGFET (Q_{ij}) whose channel is connected to a P-N-junction capacitor (C_{ij}, figures 1 and 2, structural details, figures 4 to 6 and column 5, line 53 to column 6, line 37) for storing voltages representing information;

a plurality of word lines (X_i), each coupled directly to the gates of the IGFETs of the cells in a respective row and to a selection means (X decoder) for applying a first voltage (high) and a second voltage (low) directly on said gates to select and deselect the cells in the row; and

a plurality of bit lines (B_j), each coupled to the sources of the IGFETs of the cells in a respective column and to a column select transistor (Q_5, see also column 2, last paragraph), said column select transistors being coupled to write means (via Q_8).

5.3 Although figures 4 to 6 of D4 show an N-type substrate, a P-type substrate may be used, as mentioned at lines 56 to 58 of column 5 of D4.

5.4 In the opinion of the Board, it is obvious to provide a dynamic memory device in which the memory cells each comprise a JFET in the form of a MESFET (known from D1) whose drain is connected to a capacitor in the form of a P-N-junction (known from D4). If this were implemented in accordance with the teaching of D1 and D4 with conventional techniques, the resulting DRAM device would be in accordance with Claim 1 of the second auxiliary request, for the reasons given under 3.5 and 3.6 above, and: patterned field oxide layer 30, D1, 66, D4; P-N-junction capacitor 54, 64, D4; isolated conductive region 54, D4; bit line 52, D4; channel region 56, D4; the source and drain regions would form between regions 52, 56 and 54, 56, D4 during the conventional annealing process; the metal gate 14a, D1 would form a Schottky junction with the channel; it is conventional to use polycrystalline silicon as a conductor and to apply an insulating covering layer. Since the Appellant conceded at the oral proceedings that all the details of the layers, items a) to f) of Claim 1 of the second auxiliary request, are conventional, it is not considered necessary to cite references to demonstrate this.

5.5 The Board therefore considers that the subject-matter of Claim 1 of the second auxiliary request does not involve an inventive step within the meaning of Article 56 EPC and consequently does not meet the requirements of Article 52(1) EPC.

5.6 It follows that the second auxiliary request cannot be allowed.

Order

For these reasons, it is decided that :

The appeal is dismissed.

The Registrar

S. Fabiani

S. Fabiani

The Chairman

P. K. J. van den Berg

P.K.J. van den Berg