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Bezeichnung der Erfindung:
Title of invention:
Titre de l'invention : Channel charge compensation switch with first order process independence

Klassifikation / Classification / Classement : H03K 17/16, H03K 17/14

ENTSCHEIDUNG / DECISION

vom / of / du 10 June 1988

Anmelder / Applicant / Demandeur : Hughes Aircraft Company

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Article 56

Kennwort / Keyword / Mot clé : "Inventive step (yes)"

Leitsatz / Headnote / Sommaire

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Case Number : T 105/86 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal
of 10 June 1988

Appellant : Hughes Aircraft Company
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Decision under appeal : Decision of Examining Division 068 of the European Patent Office dated 28 November 1985 refusing European patent application No. 82 304 719.6 pursuant to Article 97(1) EPC

Composition of the Board :

Chairman : P. Ford
Members : W.B. Oettinger
Y. van Henden

Summary of Facts and Submissions

I. European patent application No. 82 304 719.6, filed on 8 September 1982 claiming a priority of 29 October 1981 and published under No. 78 600, was refused by a decision of Examining Division 2.2.01.068 dated 28 November 1985.

The reason given for the decision was that the subject-matter of the independent Claim 1 and dependent Claims 2-9, filed on 1 July 1985, lacked an inventive step, having regard to the prior art represented in particular by:

(D1) US-A-4 198 580;
(D2) FR-A-2 176 129 (= GB-A-1 421 924)

and, in respect of Claims 5 and 7-9:

(D3) Don Lancaster: Das CMOS-Kochbuch, first edition 1980, IWT Verlag, pages 1-12 to 1-15 and 7-17 to 7-19.

Nothing inventive was also seen in the description or drawings.

II. On 28 January 1986 the Applicant lodged an appeal against this decision and paid the appeal fee.

He filed a statement of grounds of appeal on 4 March 1986, together with amended Claims 1-9, disputing that the Examining Division had proven the invalidity of these claims.

In particular, the assertion that arranging the transistors in a linear row, rather than in a rectangular

grid, would be obvious, is not supported by the prior art cited.

III. In response to communications from the Board, drawing attention to formal deficiencies of Claims 1 and 2, and of other documents on file, the Appellant replaced Claims 1 and 2, requested amendment of Claims 7 and 8 and replaced page 3 of the description and sheet 2 of the drawings.

The independent claim, filed on 16 April 1988, and the first dependent claim, filed on 16 April 1988 (part 1) and on 24 May 1988 (part 2), read as follows:

"1. A precision semi-conductor switch comprising: an input node (28) and an output node (30), a pair of switching transistors (20, 22) connected to the nodes, a charge retention compensating transistor (24) connected to the switching transistors, means (32, 34) connected to the gates (20c, 22c) of said switching transistors and to the gate (24c) of said compensating transistor for operating the switching transistors and the compensating transistor in complementary fashion,

each of the switching transistors (20, 22) having a source (20a, 22a) and a drain (20b, 22b) one of said source and drain being connected to said input node and the other being connected to said output node so that said switching transistors are connected in parallel with one another, said charge retention compensating transistor having a source (24a) and drain (24b) connected to a respective one of said switching transistors at one of said switching transistor source and drain,

wherein said pair of switching transistors and said compensating transistor are identically constructed on a substrate (1) with all of said transistors having said gates with nominally equal lengths and equal widths with one of the lengths and widths of said gates extending in a first dimension and an oxide layer of equal thickness so that said compensating transistor has a channel charge (Q) storage capacity equal to approximately one-half the combined channel charge storage capacity of said pair of switching transistors, characterised in that said pair of switching transistors and said compensating transistor are linearly aligned in said first dimension and all of said transistors are equally spaced and with a relative position so that the compensating transistor has a physical centroid common with that of the switching transistors (Figure 2b) whereby any linear processing variations in said first dimension of oxide capacitance and the one of the gate length and width extending in said first dimension are such that the value of any one of the oxide capacitance ($C_o + \Delta C_o$) and the one of the gate length and width ($W + W$) extending in said first dimension, of said compensating transistor is practically equal to one-half the corresponding combined value (C_o and $C_o + 2\Delta C_o$, W and $W + 2\Delta W$) of said pair of switching transistors.

2. The switch of Claim 1 further comprising a second compensating transistor (40) having a second compensating source (40a) and drain (40b) and having a gate (40c), each of said second compensating source and drain being connected to a respective one of said switching transistors (20, 22) at the other of said switching transistor source and drain, the gate of said second compensating transistor being connected to said means (32, 34) for operating said pair of switching transistors (20, 22) and the first and second compensating

transistors (24, 40) in complementary fashion, said second compensating transistor (40) being identically constructed on said substrate as the first compensating transistor (24) and said pair of switching transistors (20, 22), with said second compensating transistor having said gate (40c) with nominal equal length and equal width and an oxide layer of equal thickness to the corresponding length and width and oxide layer thickness of said first compensating transistor (24) and said pair of switching transistors (20, 22) so that said first and second compensating transistors have a combined channel charge storage capacity approximately equal to the combined channel charge storage capacity of said pair of switching transistors (Figure 2d), said second compensating transistor (40) being linearly aligned in said first compensating transistor (24) and said pair of switching transistors (20, 22), all of these transistors being equally spaced and having relative positions such that the compensating transistors (24, 40) have a physical centroid common with that of the switching transistors (20, 22) so that any linear processing variations in said first dimension of oxide capacitance and the one of the length and width of said gates extending in said first dimension are such that the combined value of any one of the oxide capacitance and the one of the gate length and width extending in said first dimension, of said first and second compensating transistors (24, 40) is practically equal to the corresponding combined value of said pair of switching transistors (20, 22)."

The remaining dependent claims concern particular features of either (Claims 4-6) the embodiment with one compensating transistor (Figure 2b) or (Claim 3) that with two compensating transistors (Figure 2c) or

(Claim 8) an embodiment with two complementary arrangements of the first kind (Figure 3) or (Claims 7 and 9) an embodiment with two complementary arrangements of the second kind (Figure 4a and 4b).

IV. The Appellant requests cancellation of the appealed decision and it follows from his submissions that he requests that a patent be granted on the basis of the following documents:

Claims 1 filed on 16 April 1988;
Claim 2, part 1 filed on 16 April 1988, part 2 filed on 24 May 1988;
Claims 3-9 filed on 4 March 1986 with clerical errors in Claims 7 and 8 corrected;
description, pages 1, 2 and 4-13 as published;
page 3 filed on 11 January 1988;
page 3a and 3b filed on 16 April 1988;
drawings sheet 1 and 3 as published;
sheet 2 filed on 16 April 1988.

Reasons for the Decision

1. The appeal complies with Articles 106-108 and Rule 64 EPC and is, therefore, admissible.

2. No objection under Article 123(2) EPC arises against the amendments made to the application documents as now on file:

2.1 Claim 1 is based on the original Claims 3 and 7, their combination and further features specifying the switch of Claim 1 being clearly disclosed in the embodiment described with reference to Figure 2a, b and c.

2.2 Claim 2 is based on the original Claims 4 and 9, their combination and further features specifying the switch of Claim 2 being clearly disclosed in the embodiment described with reference to Figure 2a and d.

Apparently, however, a clerical error occurred again on page 15a. From the previous version it follows that a few words have been omitted in the phrase bridging lines 5 and 6. The Appellant's agreement with a correction is assumed.

2.3 The dependent Claim 3 is based on the original Claim 9 and Claims 4-6 are based on the original Claims 5, 6 and 8 respectively.

2.4 The further dependent Claims 7 and 9 are based on Figure 4a and b and Claim 8 on Figure 3, including their respective descriptions.

2.5 The amendment to the description is in accordance with Rule 27(1)(c) and (d) EPC.

An obvious clerical error is found on page 8, line 14. The Appellant's agreement with its correction is assumed.

2.6 The insertion of a connection in Figure 4a removes an error which is obvious from, for instance, Figure 2a.

3. The subject-matter of both Claims 1 and 2 is not only new but, in the opinion of the Board, involves an inventive step.

This conclusion is based, essentially, on the consideration that even if a switch as known from Figure 2 of D1 is constructed in a way which is different

from Figures 3-5 of D1 but rendered obvious by D2, e.g. Figure 3, this would not result in the claimed linear transistor arrangement, and no other prior art points to a problem still unsolved and to the claimed arrangement as the solution to this problem.

The same conclusion follows for the remaining dependent claims.

All claims are therefore allowable.

More particularly, the following is pointed out:

3.1 A switch having all circuitry features of Claim 1 and Claim 2, i.e. those features which are recited in the precharacterising portion of Claim 1 until before the word "wherein" and in the first portion of Claim 2 ending with the word "fashion" are known from D1. The pair of switching transistors is represented by 23 in Figure 2 and 30-32 in Figure 3. The pair of compensating transistors is represented by 24 and 25 or 39 to 43.

Their connections are the same and this applies to the complementary operating means, too.

3.2 As its simplest implementation, Claim 1 covers, and Claim 6 specifically claims, a switch not having the second complementary transistor.

Such a circuit is not explicitly described in D1 but clearly one which must be regarded as an envisageable embodiment which allows only one of the two disadvantages of earlier switches (cf. column 1, lines 43-47) to be removed and, for this reason, has only one of the two compensating transistors (24 or 25).

3.3 This prior art double transistor (23) switch with preferably two compensating transistors (24, 25) has furthermore the constructional features recited in the second part of the precharacterising portion of Claim 1 and in the second part ending "(Figure 2d)" of Claim 2, including the resulting channel charge storage capacities.

With these features, to some extent an independence of process variations is achieved, even if D1 does not contain any statement to this effect.

This goal is, however, not fully achieved as the arrangement of the four transistors is, contrary to the statement of grounds of appeal (page 2), not rectangular, but trapezoidal; cf. page 3.

3.4 In contrast, D2 explicitly states that the effects of linear process variations of a multiplicity of paired transistors constructed on the same substrate may be eliminated.

According to D2, this goal is, contrary to the statement of grounds of appeal (page 2), fully achieved by forming the plurality of transistor pairs in a rectangular matrix arrangement. In the case of, for instance, four transistors (Figure 3) where diagonally opposite transistors are connected together (Figure 4) it is clearly true that the sum of their (different) effective capacities is the same as the sum of the (different) capacities of the other pair, given that the process variations are of a linear kind, i.e. proportional to distances, and that this is the case in both dimensions.

3.5 It would be obvious for the skilled person that he would achieve the same advantage in the switch known from D1 if

he applied the teaching of D3. Therefore he would, with the aim of obtaining full independence of process variations, consider modifying the arrangement of Figure 3 of D1 in the sense of Figure 3A of D2 by, firstly, exchanging the positions of two of the four transistors so that each of the pair 23 (30-32) and the pair 24/25 (39-43) form a diagonally disposed pair, and, second, changing the trapezoidal arrangement of the transistors (23, 25, 24, 23) into a rectangular arrangement.

3.6 However, the claimed invention differs from this obvious modification of the prior art, according to the characterising features of Claim 1 and, optionally, the third part of Claim 2 starting after "(Figure 2d)", essentially by the feature that all transistors are linearly aligned, further dimensional conditions ensuring that the linear process variations are still ineffective, despite the different arrangement.

3.7 By this difference, any difficulties arising with the precise fabrication of the rectangular matrix arrangement are circumvented.

Objectively, it can therefore be regarded as the problem to be solved by the claimed invention that the fabrication is rendered easier and/or more precise.

3.8 While this problem is, for the skilled person, an everyday problem, no incentive for solving it by leaving the principle of arranging the transistors in a rectangular matrix taught by D2, can be derived from either D2 or D1, nor from D3.

Figure 2 of D1, cannot as a schematic circuit diagram, be interpreted as teaching that the four transistors (24, 23/23, 25) should be arranged in any other way than is shown by Figure 3.

The linear four transistor arrangement claimed in Claim 2 is therefore considered to be unobvious.

3.9 The same must then apply to the three transistor embodiment claimed in Claim 1.

It may be obvious to delete, in the circuit of Figure 2 of D1, i.e. in the arrangement of Figure 3, one of the compensating transistors (24 or 25, i.e. 39/40 or 42/43), as considered in paragraph 3.2 above. But this would not result in any other arrangement than a triangle formed by the remaining transistors.

D2 does not teach anything for a three transistor arrangement, not even Figure 1.

The same applies to D3.

Order

For these reasons, it is decided that:

1. the decision under appeal is set aside;

2. the case is remitted to the first instance with the order to grant a European patent on the basis of the following application documents:

(a) Claim 1 filed on 16 April 1988,

Claim 2, part 1 filed on 16 April 1988 and part 2 filed on 24 May 1988 with the provision that on page 15a between lines 5 and 6 the words "dimension with said first" are inserted,

Claims 3-9 filed on 4 March 1986 with the provision that Claims 7 and 8 are amended as follows:
on page 16, line 30 "with" is replaced by "of",
on page 17, line 7 "each a" is replaced by ", each of the";

(b) description, pages 1, 2 and 4-13 as published with the provision that on page 8, line 14 "ΔC" is replaced by "ΔC_o",

page 3 filed on 11 January 1988,

pages 3a and 3b filed on 16 April 1988;

(c) drawings sheets 1 and 3 as published,
sheet 2 filed on 16 April 1988.

The Registrar: The Chairman:

S. Fabiani P. Ford

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