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Bezeichnung der Erfindung: A circuit for reading out address data applied to a memory in a one-chip microcomputer
Title of invention:
Titre de l'invention :

Klassifikation / Classification / Classement : G06F 1/00

ENTSCHEIDUNG / DECISION

vom / of / du 3 May 1988

Anmelder / Applicant / Demandeur : Fujitsu Limited

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence : Program counter read-out/Fujitsu

EPÜ / EPC / CBE Article 56

Kennwort / Keyword / Mot clé : Inventive step

Leitsatz / Headnote / Sommaire

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Case Number : T 169/86 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 3 May 1988

Appellant : Fujitsu Limited
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Decision under appeal : Decision of Examining Division 065 of the European Patent Office dated 6 February 1986 refusing European patent application No. 82 303 282.6 pursuant to Article 97(1) EPC

Composition of the Board :

Chairman : E. Persson
Members : J.A.H. Van Voorthuizen
P.K. Van Henden

Summary of Facts and Submissions

I. European patent application 82 303 282.6 filed on 23.06.82 (publication No. 0 069 509) claiming a priority of 25.06.81 (JP) was refused by a decision of Examining Division 065 dated 06.02.86. That decision was based on Claims 1-3 filed on 20.08.85.

II. The reason given for the refusal was that the subject-matter of the claims lacked inventive step having regard to GB-A-1 542 135 (D1), the article of Cukier et al in "IBM Technical Disclosure Bulletin", Vol. 17, No. 9, February 1975, pages 2654-2655 (D2) and US-A-3 939 452 (D3).

III. The appellant lodged an appeal against this decision by telex on 01.04.86, which telex was duly confirmed by a letter received on 07.04.86. The appeal fee was paid on 03.04.86. A Statement of Grounds was filed on 22.05.86.

IV. In the Statement of Grounds and in the course of oral proceedings held on 03.05.88 the appellant essentially argued as follows:

The problem in the present invention is to provide, without unduly complicating the 1-chip microcomputer, special means for outputting from a single pin the instantaneous contents of a program counter which, in normal operation, are not required to be supplied externally, for which no means are provided for external output, and which may be changing while the output operation is carried out. Where it has been required to investigate the contents of the program counter, the man skilled in the art used the counter overflow technique described on page 2 of the

specification, despite any knowledge of IC circuits in general which he may have acquired.

The basic technique disclosed in D1 is to count an incoming series of pulses and, in accordance with the count, to control a register output. Each register is associated with a counter; a counter ZS in Figure 2 is common to the registers SR and BFR, the counter ZR is associated with the general register REG, and the counter ZA with the accumulator AKKU. In the penultimate paragraph of the descriptive portion of the specification (lines 4 to 17 of page 4), it is stated that the same technique can be applied to output items of register information and that "the counter circuits which are already provided can also be employed for the conversion of items of register information, which consist of a plurality of bits, into pulse series which are emitted." Thus, even assuming that the contents of the program counter in the 1-chip microcomputer of the present invention were stable for the read-out period, the technique proposed in D1, involving a counter to convert the program counter content to a series of pulses, is very different from that claimed in the present invention. The shift register used in the present invention not only allows the content of the program counter to be shifted in parallel and as a whole to the shift register but also allows the instantaneous program counter content thus derived to be output as the series of binary digits which were present in the program counter at the said instant, regardless of subsequent changes in the program counter content.

With regard to D2 it was submitted that the "first register", i.e. the circuits B1 to Bn of D2 are mere buffers and are not comparable with the program counter in the 1-chip microcomputer of the present invention, which is

connected to transfer its content through the address bus to the ROM and the content of which changes continuously.

Document D3 shows the use of a shift register in serial-parallel conversion but is not otherwise relevant.

It was finally submitted that the person skilled in the art faced with the aforesaid problem would not have been led to the solution now claimed by the documents referred to.

V. The appellant requested the grant of a European patent on the basis of Claims 1-3 filed on 20.08.85, Claim 1 of which reads as follows:

1. A one-chip microcomputer including:

a program-storing read-only memory and program counter (1) both mounted on the same one-chip microcomputer, the program counter (1) having a plurality of outputs (1-1 to 1-12) for specifying reading-out addresses of the read-only memory, a program being supplied only from the read-only memory in response to the specified read-out addresses, characterized in that the one-chip microcomputer is provided with a circuit for outputting the address data read from the said program counter to an external device in order to investigate the one-chip microcomputer, the circuit comprising:

a shift register (4) comprising a plurality of stages (4-1 to 4-12), each stage having an input and an output;

a plurality of transfer gates (T_1 to T_{12}), each having an input, an output, and a gate, the inputs of the transfer gates being individually connected to respective ones of the outputs (1-1 to 1-12) of the program counter, and the outputs of the transfer gates being individually connected

to respective ones of the inputs of the stages (4-1 to 4-12) of the shift register;

an address output enable terminal (5) for receiving an address output enable signal at an arbitrary timing during the operation of the program counter, the output enable terminal being commonly connected to all gates of the transfer gates so that when the address output enable signal is applied to the address output enable terminal the transfer gates are temporarily opened by the address output enable signal and the address data stored in the program counter at that time is loaded by way of the transfer gates into respective stages of the shift register;

a single address output terminal (6) for outputting the contents stored in the shift register (4), the address output terminal being connected to the shift register output;

and in that the shift register responds to clock signals (0_1, 0_2) which are applied thereto in such a manner as to sequentially shift the loaded address data to output that address data to the single address output terminal while the program counter is operating.

Claims 2 and 3 are dependent on Claim 1.

Reasons for the Decision

1. The appeal complies with Articles 106-108 and Rule 64 EPC and is therefore admissible.

2. A one-chip microcomputer as described in the preamble of Claim 1 is generally known. It is also well known (cf. the citation on page 1 of the description) that such a one-chip

computer does not have address output terminals for outputting the contents of the program counter. Nevertheless, the requirement exists to read out these contents for investigation purposes and, according to the description, page 2, conventional program counter overflow is used therefor. The time needed to carry out this check is relatively long however.

3. Therefore, the problem to be solved was to decrease the read-out time of the program counter, without, however, adding any input/output terminals.

4. It is generally known that terminals in chips underlie severe limitations as to their number and that the use of the same terminals for multiple use requires complex multiplexing arrangements preferably to be avoided.

5. The formulation of the problem to be solved can, therefore, not be regarded as contributing to inventive step.

6. A conventional and widely used method in digital data techniques, where data which are present in parallel form have to be transmitted between separate modules but only a restricted number of terminals and/or data lines is available, consists in serialising the data before transmitting them. Examples of the use of this method in various circumstances are provided by documents D1 and D3 and by GB-A-2 023 341 (D4) cited in the European search report and commented upon by the appellant in his letter of 23.06.83.

7. In D1, page 4, lines 4-11 it is stated that "the technique of supplying items of information by means of pulse series to a module via one single-pole module terminal can also be applied to emit items of information, in particular items

of register information, from the module to other modules via one single-pole module terminal".

8. Document D4, in particular Figure 3, shows an arrangement wherein information is present in a first device in the form of parallel data, which data are serialised by means of a shift register and then transmitted to an external device via a single terminal. The external device comprises an evaluation circuit which is responsible for analysing the information.

9. Furthermore, it is generally known to use shift register means for conversion of data from parallel to serial form and vice-versa. Document D2 shows the use of such a shift register in combination with transfer gates between buffer circuits to be read out and the shift register. A common enable terminal (marked "Transfer") is connected to all the gates.

10. The Board considers that it would be obvious to the person skilled in the art confronted with the problem of reading out the contents of the program counter in a one-chip microcomputer to apply the established techniques discussed above, thereby arriving at the subject-matter of Claim 1. It has not appeared that any special difficulties had to be overcome or that any unexpected advantages have been obtained. Claim 1 is consequently to be held unallowable for lack of inventive step.

11. The dependent Claims 2 and 3 fall with the unallowable Claim 1. Moreover, the Board is unable to appreciate any inventive step in them in the light of the cited documents.

Order

For these reasons, it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

S. Fabiani E. Persson