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Veröffentlichung im Amtsblatt	Ja/Nein
Publication in the Official Journal	Yes/No
Publication au Journal Officiel	Oui/Non

Aktenzeichen / Case Number / N° du recours : T 280/86 - 3.5.1

Anmeldenummer / Filing No / N° de la demande : 81 109 554.6

Veröffentlichungs-Nr. / Publication No / N° de la publication : 0 051 870

Bezeichnung der Erfindung: Information transferring apparatus
Title of invention:
Titre de l'invention :

Klassifikation / Classification / Classement : G06F 3/04

ENTSCHEIDUNG / DECISION
vom / of / du 6 May 1988

Anmelder / Applicant / Demandeur : NEC Corporation

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Article 56

Kennwort / Keyword / Mot clé : Inventive step (no)

Leitsatz / Headnote / Sommaire

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Case Number : 280/86 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 6 May 1988

Appellant : NEC Corporation
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Decision under appeal : Decision of Examining Division 065 of the European Patent Office dated 10 April 1986 refusing European patent application No. 81 109 554.6 pursuant to Article 97(1) EPC

Composition of the Board :

Chairman : P.K.J. Van den Berg
Members : W.P.H. Riewald
R.E. Persson

Summary of Facts and Submissions

I. European patent application No. 81 109 554.6 was filed on 6 November 1981, claiming priority from a Japanese application of 6 November 1980.

The application was refused by a decision of the Examining Division dated 10 April 1986. The decision was based on Claims 1 to 5, filed with a letter of 28 January 1985, Claim 3 having been slightly amended in accordance with a letter of 18 December 1985.

The reason given for the refusal was that the subject-matter of the independent claims were considered as lacking an inventive step having regard to the prior art. Such prior art was already acknowledged in the description in connection with Figures 1, 3 and 4. The following documents reflecting the prior art were further cited during the examination proceedings:

D1: NACHRICHTENTECKNIK - ELEKTRONIK,
vol. 29, no. 6, 1979
BERLIN (DD)
W. CIMANDER et al.: "Mehrmikrorechnersysteme mit Registerkopplung"
pages 229-232

D2: ELECTRONIC DESIGN, vol. 27, no. 7,
29 March 1979
ROCHELLE (US)
D. STAMM et al.: "Free the μC's CPU from I/O hassles with a special I/O processor"
pages 102-106

D3: GB-A-2 021 823 (INTEL)

II. The Appellant filed a notice of appeal on 10 June 1986 and paid the appeal fee on the same day. On 8 August 1986 he filed, together with a statement of the grounds of appeal, new independent Claims 1 and 2, together with dependent Claims 3 to 5. The Appellant requested that the decision of the Examining Division be set aside and that a patent be granted on the basis of the new claims.

III. Oral proceedings, were held on 6 May 1988.

IV. The present independent Claims 1 and 2 read as follows:

"1. A data handling apparatus for transferring data from a transmitting unit (109) to a receiving unit (106), comprising storing means (103) for temporarily storing part of the data to be transferred, and control means (102) for controlling the data transfer by supplying, in a first cycle, a first read-command signal (IORD2) to said transmitting unit (109) to read-out first data to be stored in said storing means (103) and, in a second cycle, a second read-command signal (IORD2) to read-out second data and by supplying to said receiving unit (106) a write-command signal (MEWR2) to simultaneously write said first and second data, characterized in that said control means generates said second read-command signal (IORD2) and said write signal (MERD2 - which should obviously read MEWR2 -) in the same cycle to control said second data to be read-out and transferred from said transmitting unit (109) directly to said receiving unit (106) without being temporarily stored in said storing means (103), at the same time as said first data is transferred from said storing means (103) to said receiving unit (106).

2. A data handling apparatus for transferring data from a transmitting unit (106) to a receiving unit (109), comprising storing means (103) for temporarily storing part of the data to be transferred, a control means (102) for controlling the data transfer by supplying to said transmitting means (106) a read-command signal (MERD2) to simultaneously read-out first and second data and for storing said second data in said storing means, and by supplying to said receiving unit (109) a first write-command signal (IOWR2) to write said first data and, in a subsequent cycle, a second write-command signal (IOWR2) to write said second data, characterized in that said control means (102) generates said read-command signal (MERD2) and said first write-command signal (IOWR2) in the same cycle to control said first data to be read-out and transferred from said transmitting unit (106) directly to said receiving unit (109) without being temporarily stored in said storing means (103) at the same time as said second data is transferred from said transmitting unit (106) to said storing means (103)."

V. The Appellant argues essentially as follows:

The prior art cited in the search report exemplifies only what has already been acknowledged as prior art in the present application as filed: A data transfer between an m-bit word unit and a (2m)-bit word unit required always three cycles. One cycle is necessary in order to transfer a (2m)-bit word between the (2m)-bit unit and storage means, two cycles are necessary to transfer both m-bit words of a (2m)-bit word consecutively between the m-bit unit and the storage means. The skilled man had always in mind to store the data received from one unit entirely before sending them on to the other unit.

The invention as claimed in the independent Claims 1 and 2 (which refer to the two possible directions of data transfer) is based on the new idea that for part of the data the read-out from one unit and the write-in in the other unit are executed at the same time (i.e. in the same cycle), thereby making possible a two-cycle data transfer instead of the prior art three-cycle data transfer.

As the prior art does not give a hint to the two-cycle approach, the view of the Examining Division is regarded as a case of "ex post facto analysis". The fact that the Appellant's advantageous suggestion has not been made earlier is regarded to be an indication for an inventive step.

Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 84 EPC and is, therefore, admissible.

2. Novelty.

2.1 A data handling apparatus with the features of the preambles of claims 1 and 2 is known from D1. According to Figure 3 of this document, in connection with the appertaining description, data are transferred from an 8-bit microprocessor to a 16-bit microprocessor and vice versa. 8-bit storing means R1 and R2 are provided for the data transfer from the 8-bit microprocessor to the 16-bit microprocessor. 8-bit storing means r1 and r2 are provided for the data transfer from the 16-bit microprocessor to the 8-bit microprocessor. One 16-bit data unit is comprised of two 8-bit data units. The control of the transfer of these first and second 8-bit data from and to the 8-bit microprocessor requires two consecutive read-command signals

or write-command signals, respectively, i.e. two control cycles. The control of the simultaneous transfer of the first and second 8-bit data as a 16-bit data unit to or from the 16-bit microprocessor requires a single write-command signal or read-command signal, respectively. The said storing means provide for temporary data storage which is always necessary if at least part of the data cannot be read out from a first unit and written into a second unit at the same time, i.e. synchronously

The known control of the data handling apparatus is carried out in three cycles: two cycles for the data transfer between the 8-bit microprocessor and the storing means and one cycle for the data transfer between the storing means and the 16-bit microprocessor.

2.2 The data transfer from an 8-bit peripheral to a 16-bit physical location in a memory, disclosed in D2, page 106, left hand column, last line and right-hand column is based on a similar three-cycle approach as disclosed in D1. This can be understood from the three steps specified in the first paragraph of the said right-hand column and is confirmed by a document, filed by the applicant with a letter of 18.12.1985, which specifies the three "cycles" carried out by assembly/disassembly registers used in the 8089 input/output processor of D2.

2.3 The subject-matters of Claims 1 and 2 differ from the prior art disclosed in D1 or D2, apart from their generalised relation to first and second data of any kind, by their charcterising features which are based on the principle that the data transfer can be effected in only two cycles if part of the data transfer is carried out directly between the transmitting unit and the receiving unit, i.e. without intermediate data storage.

2.4 After examination of the further documents cited during the proceedings, the Board is satisfied that these do not disclose a prior art which comes closer to the claimed apparatus than D1 or D2. Therefore, there is no need to discuss these documents in detail.

2.5 For the above reasons the subject-matter of the independent Claims 1 and 2 is deemed to be novel within the meaning of Article 54 EPC.

3. Inventive step

3.1 Starting from the closest prior art as indicated above (D1 or D2), the objective problem underlying the two solutions specified in Claims 1 and 2, respectively, can be identified as how to increase the speed of data transfer between the transmitting and receiving devices (the two solutions concerning the two possible direction of data transfer).

There is nothing inventive in identifying this problem itself, since it is quite normal in the technical field of data handling to try to speed up the data transfer as much as possible.

3.2 When considering this problem in connection with a data transfer as disclosed in the cited prior art, the skilled man would have no difficulties to arrive at the following conclusions:

When the first and second 8-bit data, consecutively read out from the 8-bit system, are to be transmitted concurrently to the 16-bit system (Claim 1), this is, of course, only possible if both 8-bit data are available. The second 8-bit data are, at the earliest, available when they are read out in the second read cycle. So, the first 8-bit data, read out in the first read cycle, have to be stored until then. But,

there is no need to store the second 8-bit data likewise. When these are available there is, in principle, nothing which prevents passing them on to the 16-bit system directly. In other words: the skilled man will readily envisage the possibility to combine the read-command signal and the write-command signal for the said second 8-bit data in a single cycle.

Likewise, when the first and second 8-bit data, concurrently read out from the 16-bit system, are to be transmitted consecutively to the 8-bit system (Claim 2), there is, in principle, nothing which prevents passing on the first 8-bit data to the 8-bit system immediately when they are available. The skilled man will readily envisage the possibility to combine the write-command signal for the first 8-bit data with the read-command signal for the 16-bit data in a single cycle. The second 8-bit data have, of course, to be stored until the second write-command signal is given for writing the second 8-bit data into the 8-bit system.

3.3 The Board has considered the Appellant's submission that the fact that his solution has not been applied earlier despite its advantages should be regarded as an indication of inventiveness.

However, the Board has come to the conclusion that the Appellant's argument is not persuasive. The preference in the prior art for storing both 8-bit data units in a three-cycle system might be due to the great flexibility which is achieved in such a data handling apparatus rather than to any kind of prejudice against the solution on which the presnt application is based.

The data handling apparatus disclosed in D1 combines two systems with separate and independent clock systems

(page 230, right-hand column, section 3.1, third paragraph). In fact, the Appellant's suggested data handling apparatus would not be applicable in this case since in D1 there is no synchronisation of read- and write-command signals for the two separate systems.

The data input/output processor 8089 applied according to D2 is devised to perform data manipulations (such as translate and masked compare) during the data transfer. Such data manipulations appear to be not conceivable without intermediate storage of the complete 16-bit data unit (cf. D2, page 106, right-hand column, second paragraph. In passing: the meaning of the term "two cycle approach" in this paragraph appears to be not very clear in the context and is regarded not to be comparable with the two-cycle approach in the present application).

It belongs to the range of normal ability of the skilled man to envisage possibilities to simplify known data handling apparatuses. The simplification in the present case was only possible in connection with a sacrifice in flexibility, when compared with the prior art, and based on the determination of the minimum number of transfer steps in respect of the timed availability of the data. These considerations, however, are obvious for a skilled man, as set out above.

3.4 Thus, the subject-matters of Claims 1 and 2 are not considered to involve an inventive step within the meaning of Article 56 EPC and Claims 1 and 2 are, therefore, not allowable under Article 52(1) EPC.

3.5 Claims 3 to 5 are dependent on Claim 1 and for this reason also not allowable. Moreover, the Board, as the Examining Division, cannot find patentable subject-matter in any of them.

Order

For these reasons, it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

S. Fabiani P.K.J. van den Berg