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Bezeichnung der Erfindung: Non-volatile semiconductor memory device
Title of invention:
Titre de l'invention :

Klassifikation / Classification / Classement : G11C 11/34,
H01L 29/78, H01L 29/60

ENTSCHEIDUNG / DECISION

vom / of / du 28 March 1990

Anmelder / Applicant / Demandeur : Fujitsu Limited

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Article 56

Schlagwort / Keyword / Mot clé : "Inventive step (denied)"

Leitsatz / Headnote / Sommaire

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Case Number : T 310/86 - 3.5.1

DECISION
of the Technical Board of Appeal 3.5.1
of 28 March 1990

Appellant : Fujitsu Limited
1015, Kamikodanaka
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Kawasaki-shi Kanagawa 211 (JP)

Representative : S.N. Rackham
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Decision under appeal : **Decision of Examining Division 067 of the European Patent Office dated 29 April 1986 refusing European patent application No. 80 302 964.4 pursuant to Article 97(1) EPC**

Composition of the Board :

Chairman : P.K.J. van den Berg
Members : Y.J.F. van Henden
C. Payraudeau

Summary of Facts and Submissions

I. European patent application No. 80 302 964.4 (No. of publication: 0 025 311) was refused by decision of the Examining Division dated 29 April 1986.

II. The reason for the decision was that, having regard to the state of the art revealed by the documents

D1: International electron devices meeting, technical digest, 5-7 December 1977, Washington DC (US), pages 284-286, T. Ito et al. "10 write/erase, EAROM cells with directly nitrided silicon nitride films as first insulating layers",

D2: IEEE Transactions on Electron Devices, Vol. ED-24, No. 5, May 1977, New York (US), pages 547-551, Jan S. Johannessen et al. "Auger depth profiling of MNOS structures by ion sputtering",

D3: US-A-4 104 675

D4: Proceedings of the IEEE, Vol. 64, No. 7, July 1976, New York (US), pages 1039-1059, J.J. Chang "Non-volatile semiconductor memory devices",

the subject-matter of the new Claims 1-6 submitted on 28 October 1985 could not be considered as involving an inventive step.

III. The Appellant (Applicant) lodged on 12 June 1986 an appeal against the decision of the Examining Division and paid the corresponding fee on 13 June 1986. The Statement of Grounds for Appeal was received on 1 September 1986.

IV. In a communication dated 23 August 1988, the Rapporteur of the Board furthermore drew Appellant's attention to the document

D5: IEEE Journal of solid-state circuits, Vol. SC-7, No. 5, October 1972, New York (US), pages 369-375, Y. Tarui et al. "Electrically reprogrammable non-volatile semiconductor memory",

which is mentioned in (D4) as completing teachings thereof, and explained that, with regard to the content of the documents (D1), (D3) and (D4), the subject-matter of Claim 1 as refused by the Examining Division did not appear to involve an inventive step.

V. In response to the communication of the Rapporteur, the Appellant submitted new Claims 1-4 on 2 March 1989 and requested oral proceedings to be appointed if the Board intended to refuse said new claims.

VI. During oral proceedings held on 28 March 1990, Appellant's representative handed over a first set of claims numbered 1-4, replacing those received on 2 March 1989, new pages 1 and 2 of description harmonised with the claims of said first set, an auxiliary set of claims numbered 1-3 for the eventuality that the Board would refuse the first set and new pages 1 and 2 of description harmonised with the claims of the auxiliary set.

The grant of a European patent was requested on the basis of the following documents:

Claims 1-4	of the first set submitted during the oral proceedings;

Description, pages 1 and 2 harmonised with said first set of claims, page 3 received on 2 March 1989 and pages 4-7 as published with formal amendments on page 5, line 20 and page 7, line 37 as required with letter dated 24 October 1985;

Drawings, sheets 1-8 as published.

Subsidiarily, the grant of a European patent was requested on the basis of the auxiliary set of Claims 1-3 submitted during the oral proceedings, pages 1 and 2 of the description harmonised with the claims of said auxiliary set, pages 3-7 of description according to the Appellant's main request and drawings, sheets 1-8 as published.

VII. Claim 1 according to the Appellant's main request reads

"a non-volatile semi-conductor memory device of the floating-gate charge-storage type including a substrate (1) of a first conductivity type; a first insulating layer (6) on the substrate (1) the first insulating layer including silicon nitride adjacent the substrate (1); a second insulating layer (8) disposed over the first insulating layer; and floating gate charge storing means (7) located between the first and second insulating layers (6 and 8), and in which hot charge carriers generated in the substrate (1) by avalanche breakdown are injected into the floating-gate charge storing means (7) to perform a write or erase operation:
characterised in that the first insulating layer (6) also includes a layer of silicon dioxide between the silicon nitride layer and the floating gate charge storing means (7), whereby the energy band gap of the first insulating layer (6) is higher adjacent the floating gate charge

storing means (7) than adjacent the substrate (1) and decreases between them".

Claim 1 according to the auxiliary request reads

"a non-volatile semiconductor memory device of the floating-gate charge-storage type including a substrate (1) of a first conductivity type; a first insulating layer (6) on the substrate (1) the first insulating layer including silicon nitride adjacent the substrate (1); a second insulating layer (8) disposed over the first insulating layer; floating gate charge storing means (7) located between the first and second insulating layers (6 and 8), a control gate (9) disposed on the second insulating layer (8); and in which hot charge carriers generated in the substrate (1) by avalanche breakdown are injected into the floating gate charge storing means (7) with a voltage applied to the control gate (9) to perform a write or erase operation:
characterised in that the first insulating layer (6) also includes a thermally grown layer of silicon dioxide between the silicon nitride layer and the floating gate charge storing means (7), whereby the energy band gap of the first insulating layer (6) is higher adjacent the floating gate charge storing means (7) than adjacent the substrate (1) and gradually decreases between them."

The remaining claims of each set are dependent ones.

VIII. In support of his requests, the Appellant substantially argued as follows:

According to the invention, the first insulating layer of a floating gate charge storage memory device is formed of Si3N4 on the substrate and SiO2 thereover. The energy band gap of Si3N4, which is about 5 e , reduces the resistance of the layer (6) to the movement of hot electrons into the floating gate and so reduces the required write/erase voltage, whereas the SiO2 layer acts against the escape of hot electrons from the floating gate.

The cited prior art does not disclose the use of a first insulating layer with an energy band gap so graded as to be relatively low adjacent the substrate and relatively high adjacent the floating gate. Only (D3) shows a semiconductor memory device with an insulating layer having a graded energy band gap. Nevertheless, said device is of the charge trapping type and (D3) merely teaches that, where it is wished to inject charge carriers from an Al gate electrode and to prevent injection of equal and opposite charge carriers from a silicon substrate, such a layer providing a differential injection barrier may be used. Such teaching would, however, not help to overcome the problem facing the inventors, namely reducing the write-in voltage of a structure having a thick oxide film in order to achieve long term retention, as shown in (D4) and where a corresponding and opposite injection of charge carriers from the opposite side of the insulator is not liable to occur. Document (D3) furthermore fails to teach that the efficiency of a band gap decrease neither depends upon its application in a charge trapping memory device nor on the choice of a pyrolitic SiO2 as the insulating material. If the insulating layer disclosed there was used in a device according to the present invention, both carrier injection and retention would be reduced since the band gap decrease of said layer has an opposite orientation. Document (D3) finally reveals that reliability problems have been encountered with devices where a thin oxide film is overlaid with a thick Si3N4 layer. The only alternative mentioned in (D3) is thus a structure totally different from that claimed and such is also the structure known from (D2).

From document (D1), which pertains to memory devices having an insulating layer made of Si3N4 only, the skilled man learns that the latter has a lower band gap and so presents a lower threshold voltage, whereas the higher dielectric constant of Si3N4 enhances charge retention. Starting from the teachings of (D4), where floating gate devices having a relatively thick SiO2 layer are described, he would thus replace all the SiO2 by Si3N4. An additional reason for him to do so is that, having not read the present application, it would not be evident to him that the use of Si3N4 alone actually reduces charge retention and that there are conflicting requirements in the device of (D1). It is then all the more surprising that, in the invention, SiO2 is used to form part of the first insulating layer. Now, if any account was taken of the teachings in (D3), said skilled man would have to go against the specific teaching of (D1) to go back to the use of SiO2. Therefore, it is only with hindsight, and having the applicant's analysis concerning the use of a graded band gap insulator with an avalanche hot carrier injection that (D3) appears to be relevant.

Reasons for the Decision

1. The appeal is admissible.

2. Novelty.

Document (D1) pertains to non-volatile semiconductor memory devices including a silicon substrate and a stacked gate structure of which a first insulating layer is a silicon nitride film grown by thermal nitridation of the substrate - see first sentence of the abstract. Said silicon nitride film is, therefore, adjacent the substrate. Figure 1 of (D1) furthermore reveals that the substrate is of the p conductivity type - see, at the lower part of the right side, the indication "p. Si (100)" - which type of conductivity may arbitrarily be taken as first conductivity type.

Besides the silicon nitride layer adjacent the substrate, the gate structure of the memory devices comprises a floating gate and a control gate insulated from the former one by a silicon dioxide film - see page 284, last paragraph of the left hand column. As can be seen on Figure 1, the floating gate is disposed directly over the first insulating layer. This entails that the silicon dioxide layer is disposed on the other side of the floating gate, hence that the latter is located between the first and a second insulating layer, that the second insulating layer is disposed over the first one and that the control gate is disposed on the second insulating layer.

Writing and erasing are respectively achieved by injecting hot electrons and hot holes into the floating gate - see page 285, third sentence of the section headed "Writing and Erasing" - which charge carriers are generated in the substrate by avalanche breakdown - see page 284, lines 2 to 5 of the right hand column. It may thus also be asserted that the memory devices described in (D1) are of the "floating gate charge storage type". Finally, the writing and erasing operations are performed by applying a voltage to the control gate - see the left-hand column of page 285, lines 7 to 13 of the first paragraph.

The first insulating layer being exclusively made of silicon nitride and no band gap grading mentioned, the subject-matter of Claim 1 according to either of Appellant's requests is novel with respect to the disclosure of (D1). Among the other cited documents, only (D3) reveals the use of an insulating layer with a graded band gap. Said layer is, however, provided in a charge trapping memory device, so that (D3) and the remaining documents are considered to be less relevant for the purpose of assessing novelty.

3. Inventive step.

3.1 It is stated in (D1) that, by using silicon nitride instead of silicon dioxide for making the first insulating layer, a reduction of write/erase voltages, an improvement of charge retention owing to the higher dielectric constant of silicon nitride and, owing to its narrower band gap, an enhancement of carrier injection into the floating gate are achieved - see page 284, last fifteen lines of the right-hand column, and page 285, lines 4 to 6 of the summary.

Such statements must, however, not be interpreted to the letter. In floating gate memory devices, the charge storing element is the capacitor formed by the substrate, the first insulating layer and the floating gate. Now, every one skilled in the art knows that the charge retention of a capacitor depends on the resistance its dielectric layer opposes to electron migration from the negative plate to the positive one, i.e. on the electrical resistivity of the dielectric material and not on the dielectric constant of said material. It is also known that, when a capacitor is being charged, the amount of charges moving from one plate to the other one is limited by the capacity of said capacitor and by the applied voltage. Therefore, the higher the dielectric constant of the insulating layer, the greater the stored charge.

It may not be denied that, all other conditions remaining unchanged, the higher the charge initially stored in a floating gate is, the longer the part thereof retained in the gate will represent an exploitable information. This may be the reason why the authors of (D1) concentrated on the dielectric constant rather than the resistivity of silicon nitride and, from the conclusion of their article, it appears that they expected fairly long retention times - see last but one sentence of the summary. Nevertheless, as may be inferred from Appellant's statement that the use of silicon nitride alone actually reduces charge retention, experimental results obviously fell short of these expectations and the need of improving the memory devices described in (D1) was felt without more ado.

Therefore, no inventive step can be perceived in defining the task which the present invention sets out to meet.

3.2 The floating gate memory devices described in document (D4) are provided with insulating layers made of silicon dioxide - see Part III. It is revealed there that the advantage of such devices is a long retentivity, whereas their disadvantage is the need of large power amounts for writing and a difficulty to erase - see page 1049, last paragraph of the right-hand column. In particular, the need of a high positive control gate bias, typically 60 volts, for switching the device to a high threshold voltage is mentioned - see page 1050, lines 12 to 14 of section III.D.

In contrast thereto, emphasis is laid in (D1) on a reduction of write/erase voltages to 10 volts which is achieved by using, in floating gate memory devices, silicon nitride as constituent material of the first insulating layer - see last paragraph of the introduction. Therefore, bearing in mind that (D4) presents a review of the memory devices which were known at the time it was drafted, and that the content of (D1) was made available to the public about one and a half years later than that of (D4), the skilled man readily understands that (D1) gives account of an attempt to improve over the state of the art known from (D4).

3.3 The task of the technician involved in the design and fabrication of floating gate memory devices is to steadily improve such devices. Therefore, having discovered the drawbacks of the devices disclosed in (D1), his attitude should not be, as the Appellant nevertheless contends, to go back to the solutions reviewed in (D4) but to look for something else.

A first course open to the skilled man seeking to improve floating gate memory devices and starting from the state of the art revealed by (D1) and (D4) might be to inform about the availability of better dielectric materials. The list of dielectric materials suitable for making insulating layers in semiconductor devices with a silicon substrate is, however, rather short. Furthermore, it may not be denied that the use of silicon nitride for making the first insulating layer of a floating gate memory device exhibits advantages over that of silicon dioxide. Therefore, without having to display inventiveness, said skilled man is quite naturally induced to examine whether a compromise can be found between the solutions respectively known from (D1) and (D4).

3.4 From document (D3), the skilled man learns that, in semiconductor devices comprising an insulator at one interface of which holes or electrons are to be injected, the provision of a graded band gap promotes carrier injection from said interface under the action of a moderate electric field while, simultaneously, electron or hole injection from the opposite interface is blocked - see the first six lines of column 1. The generality of this teaching is stressed by the implicit reference to a category of semiconductor devices characterised by such a band gap structure. In relation with a charge trapping memory device comprising a silicon substrate, a layer of silicon dioxide and an aluminum contact, (D3) furthermore teaches that by reducing the band gap of the insulator layer near the aluminum - silicon dioxide interface, holes or electrons can be injected from the aluminum into the insulator, the injection of electrons or holes from the opposite silicon - silicon dioxide interface being blocked - see lines 3 to 10 of column 3.

It is, however, obvious that charge carrier injection cannot be influenced by the fact that the injected carriers will remain in the bulk of the insulating material, i.e. be trapped, or will gather on a floating gate. Likewise, no difference either can result from the fact that said carriers are already available, as are the free electrons of an aluminum contact, or that they are generated by avalanche breakdown in a semiconductor just before an electric field is applied to drive them into the insulator. Therefore, even if the skilled man might be assumed to ignore the opportunity of providing, in charge storage memory devices, a graded band gap insulating layer having its narrowest band gap on that side where charge carriers are to be injected, said opportunity, as well as its interest in the case of floating gate memory devices, would anyway become obvious to him.

3.5 Now, it is true that, as the Appellant pointed out, reliability problems are said in (D3) to have been encountered with memory devices in which a thick silicon nitride film covers a thin silicon dioxide layer formed on a silicon substrate - see column 1, lines 32 to 61. Said devices, however, are MNOS memory FETs in which charge carriers are driven from the silicon substrate into the insulator layer and trapped in the silicon nitride - see also page 1040 of (D4), figures and first two paragraphs of the section headed "MNOS". In these devices, the band gap of the insulating layer is the broadest on that side where charge carriers are to be injected. It thus appears that the above mentioned shortcoming is not liable to deter the skilled man from providing, in a floating gate memory device, a silicon nitride film adjacent a silicon substrate and a silicon dioxide film between said silicon nitride film and the floating gate. As a matter of fact, this shortcoming much more represents an incentive to do so.

3.6 With regard to the preceding, the exercise of inventive ingenuity appears not to be needed to provide, in a memory device of the kind disclosed in (D1), a silicon dioxide film between the floating gate and the silicon nitride film adjacent the silicon substrate. This measure entailing a band gap decrease in the direction from the floating gate towards the substrate, no inventive step can thus be perceived in the subject-matter of Claim 1 according to the Appellant's main request - Article 56 EPC.

No inventive ingenuity either is required to make the band gap decrease to be gradual since both the principle and the advantages of this measure are disclosed in (D3) - see the figures 2, 3 and column 3, lines 3 to 19 - or to produce the silicon dioxide layer by thermal growing, i.e. a method widely carried out while making semicoductor devices and advisable in the present case. Therefore, the subject-matter of Claim 1 according to the Appellant's auxiliary request also lacks an inventive step - Article 56 EPC.

4. Claim 1 according to either of Appellant's requests is not allowable - Article 52(1) EPC.

Order

For these reasons, it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

M. Beer P.K.J. van den Berg