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Bezeichnung der Erfindung: A semiconductor integrated circuit device
Title of invention:
Titre de l'invention :

Klassifikation / Classification / Classement : H01L 27/08, H01L 29/10

ENTSCHEIDUNG / DECISION
vom / of / du 6 October 1988

Anmelder / Applicant / Demandeur :

Patentinhaber / Proprietor of the patent /
Titulaire du brevet : Fujitsu Limited

Einsprechender / Opponent / Opposant : I. Deutsche ITT Industries GmbH
II. Siemens AG

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Article 56 EPC

Schlagwort / Keyword / Mot clé : Non-inventive sequential analogue uses

Leitsatz / Headnote / Sommaire

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Case Number : T 178/87 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal
of 6 October 1988

Appellant : (Opponent 01)
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Decision under appeal : Decision of the Opposition Division of the European Patent Office dated 12 February 1987 rejecting the opposition filed against European patent No. 0 033 028 pursuant to Article 102(2) EPC.

Composition of the Board :

Chairman : K. Lederer
Members : H. Reich
G. Paterson

Summary of Facts and Submissions

I. European patent 0 033 028 was granted on the basis of European patent application No. 80 303 928.8. The patent comprises five claims, of which Claim 1, the sole independent claim, reads as follows:

"1. A semiconductor integrated circuit device, including short channel MOS transistors, having an input circuit and an internal circuit, characterised in that the channel length of a first-stage transistor of the input circuit is greater than the channel lengths of transistors of the internal circuit."

II. The Appellants separately filed notices of opposition and requested revocation of the patent in its entirety on the ground of non-patentability in view of the prior art disclosed in particular in the following documents:

DE-A-2 458 226 (D1);
US-A-3 731 161 (D2); and
IBM Technical Disclosure Bulletin, Vol. 12, No. 9, February 1970, page 1391 (D3).

III. The Opposition Division rejected the opposition, holding that the subject-matter of Claim 1 was novel and involved an inventive step, since the cited prior art documents neither disclosed, nor hinted at, the provision of a first stage transistor of an input circuit having a greater channel length than the transistors of an internal circuit in an integrated circuit device. In particular, document D2 would disclose to provide an input transistor with a thicker gate insulation film than the transistors of the internal circuit as a means primarily for reducing at the input the likelihood of a short-circuit of the gate

insulation. For this reason, a skilled person would never think of replacing the thick gate insulator film of the input transistor by a channel of increased length such as known from document D3 and arrive at the subject-matter of Claim 1 in an obvious way.

IV. Both Appellants (Opponents) lodged an appeal against the decision.

V. Oral proceedings were held before the Board, at the end of which both Appellants requested that the decision under appeal be set aside and the patent be revoked.

The Respondent (Proprietor of the patent) requested that the appeals be dismissed.

VI. In support of their request, the Appellants essentially submitted that the subject-matter of Claim 1 failed to involve an inventive step. In circumstances in which gate insulation shorting is not to be expected in practice, it would be obvious for the skilled person to replace the thick gate insulation film technique, which is disclosed in document D2 as a means for increasing the threshold voltage of input transistors in order to improve the input noise margin, by the provision of longer channels which measure document D3 explicitly teaches to increase the threshold voltage. The more so, since the latter technique has the readily foreseeable advantage of being easier to realise.

VII. These arguments were contested by the Respondent, who essentially made the following submissions:

(a) Document D3 merely discloses the effect of short channels on the threshold voltage of insulated gate field effect transistors without dealing with the

input noise margin problem to which the present invention affords a solution.

(b) Document D1 is dedicated to a different problem, i.e. reducing the output impedance of a semiconductor device comprising field effect transistors and for this purpose, teaches to provide short channel transistors only in the output stage of the device.

(c) Document D2 discloses to use input field effect transistors of an integrated circuit with a thicker gate insulation not only for enhancing the circuit's tolerance to input noise voltages but also for reducing the likelihood of gate insulation shorting. A skilled person would intend to keep the advantage of puncture strength. He would therefore not depart from the thick gate insulation design in document D2 in order to use instead the claimed long channel structure known from document D3, which is not capable of providing any protection against a gate insulation shorting.

(d) Document D3 has already been published in 1970, i.e. about 18 months before the thick gate oxide technique described in document D2 was filed. Also, document US-A-4 156 939 (D4) filed about eight years after the publication of document D2 does not use longer channels but teaches to provide the transfer channel of a memory cell IG FET with a higher impurity concentration for increasing that IG FET's threshold voltage and rendering it thus insensitive to noise pulses.

These facts would provide evidence that the use of the long channel technique known from document D3 for increasing the input noise margin was not obvious.

Non-obviousness of the claimed subject-matter is evidenced also by the nine years period extending between the date of availability of the teaching of document D3 and the priority date of the present invention. Such a period is to be regarded as very long in a technological field under so rapid and considerable development.

Reasons for the Decision

1. The appeal is admissible.

2. Novelty.

2.1 Document D1 discloses "a semiconductor integrated circuit device, including short channel MOS transistors (see D1, page 4, lines 6-10)", having an output circuit (20, 30 in Figure 1) and a further integrated circuit (10 in Figure 1), see page 3, second paragraph. The "further integrated circuit" must necessarily include some input circuit. Otherwise, the whole device could not function.

The Board is, further, convinced, that the definition of a "short channel transistor" as a transistor with a channel length within the region in which the so called "short-channel-effect" renders the threshold voltage dependent on the length of the channel, is generally accepted in the field in question. Moreover, it is generally known in the field of FETs that the decrease of the threshold voltage starts at 5μm in the direction of smaller lengths; see for instance document D3, Figure 1B. Thus, the known channel lengths of 5μm and 1μm (D1, page 4, line 9) and the explicit channel lengths of less than 3μm mentioned in the present patent belong both to "short channel transistors".

The above-mentioned features of the device known from document D1 therefore correspond to the features of the precharacterising part of Claim 1. The length condition defined in the characterising part of Claim 1 is not derivable from document D1. In document D1 the channel lengths of input- and internal-transistors are not explicitly stated but can be interpreted to be identical, see D1, page 4, lines 1-5.

2.2 Document D2 discloses a semiconductor integrated circuit device including MOS transistors and having an input circuit (1 in Figure 1) and an internal circuit (2). Contrary to the subject-matter of Claim 1, these known MOS transistors are not of the short channel type, and the channel length of the first stage transistor 1 of the input circuit (12,5μm) is shorter than the channel length of the transistor 2 of the internal circuit (75μm; column 3, lines 16 to 29).

2.3 Document D3 shows that the threshold voltage of a single short channel insulated gate field effect transistor decreases with its channel length (Figure B). It further teaches that by differently spacing the diffusions in two different devices on the same substrate, a different threshold voltage can be obtained in each device (page 1391, last sentence). However, this document does not specify to which portions of a given device with input and interior circuits such different channel lengths should be allocated respectively.

2.4 The remaining documents on file do not come closer to the subject-matter of Claim 1.

2.5 For the above reasons, the subject-matter of Claim 1 is considered to be novel within the meaning of Article 54 EPC.

3. Inventive step.

3.1 Starting from the nearest prior art as disclosed in document D1, the objective problem underlying the present invention as claimed in Claim 1 is to improve in an integrated circuit device, including short channel transistors, the admissible noise margin of its input circuit transistors.

3.2 When following the well known development direction in the art of integrated circuits to enhance the integration density, a skilled person will find out in practice that the reduction of the channel lengths, related to this miniaturisation leads to an undesirable reduction of the input noise margin that can be admitted without that any erroneous operations of circuit components occur. Therefore, no positive contribution to inventive step can be seen in formulating the technical problem.

3.3 The problem mentioned in point 3.1 above is solved according to the characterising part of Claim 1 by the following dimensioning rule for the channel length L:

L (input circuit) > L (interior circuit).

Thus, it remains to consider whether it is obvious to a skilled person to use such a dimensioning rule for an improvement of the noise margin.

3.4.1 Although the channel length of the transistors described in document D2 is substantially longer (12μm) than the channel length (2 to 3μm) of the transistor according to the patent in suit the Board regards a skilled person to be able to draw from this document the <u>general</u> teaching that

independently of the channel length of the transistors used, in a circuit comprising insulated gate field effect transistors the tolerance to the input noise level can be increased by increasing the threshold voltage of the transistors connected to the input terminals of the circuit. (D2, Claim 1; column 1, lines 11 to 21). Thus, a skilled person knew at the priority date of the patent in suit which parameter of which transistor in a circuit as known from D1 he has to change and in which way in order to arrive at his intended aim.

3.4.2 Thus, the above mentioned problem (how to increase the noise margin) boils down to the problem of how to increase the threshold voltage of some of the short-channel insulated gate field effect transistors of an integrated circuit device.

3.4.3 It is known from document D3 that the threshold voltage of short-channel insulated gate field-effect transistors can be increased by increasing their channel length and that different thresholds can be obtained for two different devices formed in the same substrate by selectively spacing the diffusions (page 1391, last sentence), i.e. by producing channels of different length.

The Board is satisfied that a skilled person would take advantage of these known facts and, therefore, would make the channel length of a first-stage transistor of an input circuit greater than the channel length of transistors of the internal circuits of an integrated circuit device built up with insulated gate field effect transistors in order to increase the noise margin of the input circuit. This all the more as a skilled person is able to foresee the advantage of the known channel length variation technique according to document D3 over the use of different thicknesses as disclosed in document D2 because it requires

less manufacturing steps, since the different channel lengths may be simultaneously defined on the substrate whereas different gate insulation thickness calls for additional masking, deposition and oxidation steps (see also document D2, column 4, lines 44 to column 5, line 22).

3.4.4 On the other hand, the channel length variation technique does not allow to simultaneously increase both, the threshold voltage and the puncture voltage as the gate oxide thickness variation technique does. This disadvantage being foreseeable, the Respondent cannot be followed in his view that the replacement of gate insulation thickness technique by the channel length technique implies an inventive step. It must remain open for a skilled person to evaluate whether for his particular purposes the advantage of less manufacturing steps outweighs the disadvantage of no additional puncture voltage increase.

3.5 Neither could the Respondent's submissions that the early teaching from document D3 had not been implemented in any of the devices disclosed in later documents D2 and D4, and that it had been available for a relatively long period before the present invention was actually made (point VII(d)), lead the Board to reach a different conclusion. For documents D2 and D4 do not specifically relate to the type of semiconductor integrated circuits including <u>short channel MOS transistors</u> to which the present patent is dedicated and for which variations of the channel length of certain transistors can markedly affect the value of the threshold voltage. In addition, the known devices to which these documents relate, clearly involve specific aspects which indeed may justify the selection of a different technique for increasing the threshold voltages: In particular, the device of document D2 is intended to handle and withstand as well higher operating voltages, which

explains preference of the thick gate insulation technique. Document 4 is dedicated to the problem of increasing the threshold voltages of the transfer gate in each internal memory cell of an integrated semiconductor memory device. A normal memory chip comprising mainly memory cells, an increase of the channel length of all transfer gates instead of varying their impurity concentration would destroy the advantage of a higher integration density deriving from the use of the short channel technology.

Neither did the Respondent convincingly establish the existence of a long felt want before the invention was actually made, since he did not demonstrate that, throughout the nine years period referred to, short channel MOS integrated devices had already gained substantial practical significance and that they had been subject to constant and unfruitful investigation in order to solve the technical problem underlying the invention, nor did he even seek to do so.

3.6 The Respondent's argument mentioned in point VII(b) above lies outside the frame of the Board's reasoning of lack of inventive step.

3.7 As shown in detail above, in order to arrive from the prior art at the subject-matter of Claim 1, a skilled person only has to apply in the device known from document D1 the known theoretical teaching derivable from document D2 - that the noise margin can be improved by a higher threshold voltage - and to realise technically such higher threshold voltage by the channel length variation technique known from document D3. Both steps are held to be obvious per se.

For these reasons, the subject-matter of Claim 1 is considered to lack an inventive step within the meaning of Article 56 EPC, and it is therefore not patentable (Article 52 EPC).

3.8 Claims 2-5 are dependent on Claim 1 and, therefore, not patentable either.

4. Accordingly, the ground of opposition set out in Article 100(a) EPC prejudices the maintenance of the European patent.

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.

2. The European patent is revoked.

The Registrar: The Chairman:

F. Klein K. Lederer