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Bezeichnung der Erfindung: Offset compensation for switched capacitor  
Title of invention: integrators  
Titre de l'invention :

Klassifikation / Classification / Classement : G06G 7/186

**ENTSCHEIDUNG / DECISION**

vom / of / du 7 November 1989

Anmelder / Applicant / Demandeur : American Microsystems Incorporated

Patentinhaber / Proprietor of the patent /  
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPU / EPC / CBE Article 56 EPC

Schlagwort / Keyword / Mot clé : "Inventive step - yes"

**Leitsatz / Headnote / Sommaire**

Europäisches  
Patentamt

Beschwerdekammern

European Patent  
Office

Boards of Appeal

Office européen  
des brevets

Chambres de recours



Case Number : T 335/87 - 3.5.1

**D E C I S I O N**  
of the Technical Board of Appeal 3.5.1  
of 7 November 1989

**Appellant :** American Microsystems Incorporated  
3800 Homestead Road  
Santa Clara  
CA 95051 (US)

**Representative :** Martin, Jean-Jacques  
Cabinet REGIMBEAU  
26, Avenue Kléber  
F-75116 Paris (FR)

**Decision under appeal :** Decision of Examining Division 066  
of the European Patent Office  
dated 10 April 1987 refusing European  
patent application No. 82 401 372.6  
pursuant to Article 97(1) EPC

**Composition of the Board :**

**Chairman :** E. Persson  
**Members :** W.J.L. Wheeler  
W. Riewald

## Summary of Facts and Submissions

- I. Appellant's European patent application No. 82 401 372.6, filed on 23 July 1982, claiming priority from a previous application US 287 387 of 27 July 1981, was refused by a decision of the Examining Division dated 10 April 1987. That decision was taken on the basis of Claims 1 and 2 as originally filed and Claims 3 to 6 filed with a letter dated 13 February 1986.
- II. The reason given for the refusal was that the subject-matter of the claims did not involve an inventive step within the meaning of Article 56 EPC having regard to the following prior art documents:
  - D1: Wescon Conference Record, 16 - 18 September 1980, Anaheim CA, USA, pages 26/1, 1 - 14;
  - D2: BE-A-887 045;
  - D3: IEEE Transactions on Circuits and Systems, Vol. CAS-27, No. 6, June 1980, pages 515 - 521.
- III. On 9 June 1987 the Appellant filed a Notice of Appeal against that decision. The fee for appeal was paid on the same day. The Statement of Grounds was filed on 10 August 1987.
- IV. In reply to a communication from the Board, the Appellant filed with a letter dated 2 October 1989 (received on 4 October 1989) new Claims 1 to 3 and replacement pages of description.

V. The Appellant requests that the decision under appeal be set aside and a patent granted on the basis of the following documents:

- Claims 1 to 3, filed on 4 October 1989, and Claims 4 to 6, filed with the letter dated 13 February 1986, received on 17 February 1986;
- Description: pages 1, 4, 6, 7 and 14, filed on 4 October 1989, and pages 2, 3, 5 and 8 to 13 as originally filed;
- Drawings, sheet 1/2, filed on 17 February 1986, and sheet 2/2 as originally filed.

VI. Claim 1 is now worded as follows:

"1. An integrator containing an integrator input terminal (10) and an integrator output terminal (21) comprising an operational amplifier (19) having an inverting input lead (17), a non inverting input lead (18) and an output lead (20), said operational amplifier (19) producing an offset voltage on said output lead (20), a first switch means (33) responsive to a first phase ( $\phi_1$ ) of a signal having two phases, said first switch means (33) connected between said inverting input lead (17) and said output lead (20), a first capacitor (23), having a capacitance  $C_1$ , having a first and a second plate, said first plate being connected to said inverting input lead (17) of said operational amplifier, a second switch means (24), responsive to a second phase ( $\phi_2$ ) of said signal having two phases, said second switch means (24) being connected between said second plate of said first capacitor (23) and said output lead (20) of said operational amplifier, and switched capacitor means (11-16) connected between said inverting input lead (17) and said integrator input terminal (10),

said switched capacitor means serving as a resistor equivalent and including a third capacitor (16) having a first and a second plate, said third capacitor having capacitance  $\alpha_1 C_1$ , whereby the effect of said offset voltage on the integrator output voltage available on said output terminal is eliminated by the simultaneous integration of said input voltage and said offset voltage during the period when said first clock phase is low and said second clock phase is high, said integrator characterized by further comprising:

- a second capacitor (28), having capacitance value  $\alpha_2 C_1$ , having a first and a second plate, said first plate connected to said inverting input lead (17) of said operational amplifier;
- third switch means (32), responsive to said second phase ( $\phi_2$ ), said switch means connected between said second plate of said second capacitor (28) and said output lead (20) of said operational amplifier; and
- a fourth switch means (29), responsive to said first phase ( $\phi_1$ ), said fourth switch means connected between said second plate of said second capacitor (28) and a voltage reference, said second capacitor, third switch means and fourth switch means forming a switched capacitor resistor of a lossy integrator."

Claims 2 to 6 are dependent on Claim 1.

#### Reasons for the decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is, therefore, admissible.

2. All the features specified in the current Claims 1 to 6 are in the originally filed Claims 1 to 6 respectively, except for: (a) the explicit mention at the end of Claim 1 that the second capacitor and the third and fourth switch means form a switched capacitor resistor of a lossy integrator, which is disclosed at the top of page 10 in the originally filed description, and (b) the recital in Claim 4 that the seventh switch means is connected between the voltage reference and the second plate of the first capacitor, which is disclosed on page 8, lines 19 to 22, in the originally filed description.

The amendments made to the description and the amendment made to Fig. 3 of the drawings are only for the purposes of adapting the description to the current Claim 1, indicating the prior art, and removing inconsistencies.

Therefore the current version of the application does not contravene Article 123(2).

3. As now acknowledged on page 7 of the present application, the closest prior art is known from D1, Fig. 9 of which shows a switched capacitor amplifier with a first stage according to the prior art portion of Claim 1.
4. The integrator according to Claim 1 differs from the prior art known from D1 in having an additional feedback branch comprising a capacitor having a first plate connected to the inverting input of the operational amplifier and a second plate connected to the output of the operational amplifier via third switch means, responsive to said second phase, and a fourth switch means, responsive to said first phase, connected between the second plate of said capacitor and a voltage reference, said capacitor and third and fourth switch means forming a switched capacitor resistor of a lossy integrator.

5. The Board accepts the Appellant's explanation that the additional feedback branch is not provided to compensate for the offset voltage of the operational amplifier. Such compensation is already achieved by the features in the prior art portion of Claim 1, as is explained under the heading "SWITCHED CAPACITOR AMPLIFIERS" on pages 9 and 10 of D1. This may also be deduced from equation (5) on page 10 of the present application, since the terms in  $V_{OFF}$  in the first and third lines of the equation mutually cancel. As is explained on page 10 of the present application, the additional feedback branch provides resistive feedback to achieve a lossy integrator possessing a transfer function desired for a particular purpose. This is done in such a way that the compensation for the offset voltage of the operational amplifier is retained, as can be seen from equation (5), where the terms in  $V_{OFF}$  in the second line of the equation mutually cancel.
6. Although, at first sight, there appears to be a certain similarity between the feedback loop (20) shown in Figs. 4, 5 and 6 of D2 and the additional feedback branch as specified in the characterising portion of Claim 1 of the present application, the Board notes that the function and method of operation of the additional feedback branch of the present application is quite different from that of the feedback loop (20) described in D2 from page 7, line 32 onwards. In D2, a first switch (22) connects the output of an operational amplifier (12) to a line connecting its negative input to one plate of a capacitor (24), the other plate of which is connected by a second switch (26) to ground (as shown in Fig. 4) to charge the capacitor (24) to the offset voltage of the amplifier. Then the first switch (22) is opened while the second switch (26) still connects the other plate of the capacitor (24) to ground

(as shown in Fig. 5). Later, the second switch (26) is switched to connect the other plate of the capacitor (24) to the output of the amplifier (as shown in Fig. 6). Thus in D2 the switches (22, 26) are not operated in phase. On the other hand, according to Claim 1 of the present application, the first and fourth switch means are responsive to the first phase of a signal having two phases and the third switch means is responsive to the second phase of the signal having two phases. The Board has found no hint in D2 that the switches (22, 26) could be operated in the manner specified in Claim 1 of the present application for the "corresponding" first, third and fourth switch means, or that the loop (20) could serve as a switched capacitor equivalent of a feedback resistor in a lossy integrator.

7. In the opinion of the Board, the disclosure in D2 would not lead a person skilled in the art to modify the circuit shown in Fig. 9 of D1 in such a way as to arrive at the integrator claimed in Claim 1 of the present application.
8. In the opinion of the Board, D3 and the other documents cited in the European search report are less relevant than D1 and D2.
9. In the result, the Board takes the view that the lossy integrator claimed in Claim 1 of the present application is not obvious having regard to the cited prior art and therefore involves an inventive step within the meaning of Article 56 EPC.
10. Claims 2 to 6 are properly dependent on Claim 1. It follows that their subject-matter also involves an inventive step.

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.
2. The case is remitted to the first instance with the order to grant a patent on the basis of the Appellant's request (paragraph V above).

The Registrar:

*S. Fabiani*

S. Fabiani

The Chairman:

*E. Persson*

E. Persson