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Bezeichnung der Erfindung: / Title of invention: / Titre de l'invention : Semiconductor integrated circuit device with output stage

Klassifikation / Classification / Classement : H01L 27/08

ENTSCHEIDUNG / DECISION
vom / of / du 7 July 1988

Anmelder / Applicant / Demandeur : Fujitsu Limited

Patentinhaber / Proprietor of the patent / Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Article 56 EPC

Schlagwort / Keyword / Mot clé : "Inventive step (yes)"

Leitsatz / Headnote / Sommaire

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Case Number : T 369/87 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 7 July 1988

Appellant : FUJITSU LIMITED
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Decision under appeal : Decision of Examining Division 048 of the European Patent Office dated 24 April 1987 refusing European patent application No. 83 307 727.4 pursuant to Article 97(1) EPC

Composition of the Board :

Chairman : K. Lederer
Members : E. Turrini
G. D. Paterson

Summary of Facts and Submissions

I. European patent application 83 307 727.4 (publication number 0 114 491) was refused by a decision of the Examining Division.

II. The reasons given for the refusal were that Claims 1 and 3 of the effective set of claims as filed on 29 September 1986 did not satisfy the requirements of Article 123(2) EPC, since they contained subject-matter which was not disclosed in the application documents as originally filed.

It was further stated in the decision that any new Claim 1 which would be reduced to its originally disclosed subject-matter would not satisfy Article 56 EPC. The reason for this was that the original Claim 1 was considered to define an obvious use of the technique known from the document DE-A-3 107 543 (D1) in a closely analogous situation, as could be seen from earlier communications of the Examining Division referred to in the decision.

III. The Appellant lodged an appeal against this decision.

IV. Oral proceedings were held on 7 July 1988 at the end of which the Appellant requested that the decision of the Examining Division be set aside and a European patent granted on the basis of an amended set of application documents as handed over during the oral proceedings.

The effective set of claims comprises two claims, of which Claim 1, the sole independent claim, reads as follows:

"1. A semiconductor integrated circuit device comprising a first MIS FET (3, 4, 12, 16) for forming an internal

circuit for a device operating at a standard voltage of 5 volts and a second MIS FET (3, 4, 12, 17) which is adapted to receive a voltage higher than the standard voltage, the second MIS FET (3, 4, 12, 17) having a channel length (L_2) greater than that (L_1) of the first MIS FET (3, 4, 12, 16) and having a gate insulator (17) thickness greater than that (16) of the first MIS FET (3, 4, 12, 16), characterised in that the second MIS FET forms an output stage circuit directly coupled to an external voltage source of 12 volts, the second MIS FET (3, 4, 12, 17) providing a reduced drain current characteristic at a drain voltage substantially lower than its drain breakdown voltage."

Claim 2 is appended to Claim 1.

VI. In support of the allowability of his request, the Appellant argued substantially as follows:

The invention relates to the direct coupling of a semiconductor integrated circuit, which comprises a first MIS FET forming an integral circuit operating at a standard voltage and a second MIS FET forming an output stage circuit, to an external device driven by a voltage higher than the standard voltage but still substantially lower than the drain breakdown voltage of the second MIS FET. If, due for example to fluctuations in the integrated circuit manufacturing process, the channel length of the second MIS FET is shorter than a predetermined length, a so-called "punch-through" effect occurs that increases the drain current for a specific voltage and, consequently, lowers the junction sustaining voltage, which is defined as a voltage value at which the junction allows a drain current of 1μA under the gate bias voltage of zero.

Reduction of this leak-like current has been achieved by the prior art "offset gate" structures wherein the drain region is separated from the gate region via an additional low concentration region, which amounts to inserting an extra-resistor therebetween. Manufacturing such structures, however, requires additional process steps and results in lower yields of chips per wafer.

It has now been found that the junction sustaining voltage of the second MIS FET can be increased by increasing the thickness of the gate insulator layer, and that simultaneously increasing its channel length provides a supplementary "safety net" against possible fluctuations during mass production of the integrated circuit.

Whilst it is admitted that the technical measure consisting of simultaneously increasing the gate insulator layer and the channel length of a MIS FET was known already from the prior art, such measure served a different purpose and its interest for enhancing the junction sustaining voltage of a MIS FET forming an output stage circuit of an integrated circuit was not predictable.

In particular, document D1 relates to an EPROM integrated circuit which comprises MIS FETs operating at 5 volts and further MIS FETs in the peripheral circuit portion which are to stand write voltages as high as 25 volts. The breakdown voltage of the latter MIS FETs is increased by simultaneously increasing the thickness of their gate insulator layer and their channel length. There is no suggestion in this document that such MIS FETs also exhibit a reduced drain current characteristic at a drain voltage which is far away from the breakdown voltage and that they could advantageously form output stages circuits for direct coupling to an external source of such relatively low voltage.

Reasons for the Decision

1. The appeal is admissible.

2. There is no objection under Article 123(2) EPC to the present application documents, since they are adequately supported by the application documents as originally filed.

In this respect, present Claim 1 is distinguished from Claim 1 as originally filed essentially in that the internal circuit formed by the first MIS FET is specified to operate at a standard voltage of 5 volts and in that the second MIS FET is specified to be directly coupled to an external voltage source of 12 volts and to provide a reduced drain current characteristic at a drain voltage substantially lower than its drain breakdown voltage. These amendments are supported by the statement in the original description of the general desire, which is implicitly met by the invention, to directly couple a semiconductor operating with a standard 5 volts power source to an apparatus driven by a 12 volts power source (page 1, lines 7 to 12), by the indication that the output-stage MIS FET according to the invention is "for the direct coupling with the 12 volts system" (page 6, lines 1 to 3) and by the description made with reference to Figure 1 of the influence that the "punch-through" phenomenon would exert on the drain current and drain junction sustaining voltage if not overcome by the invention, wherein furthermore avalanche breakdown is explicitly stated to occur at much higher voltages (page 3, lines 17 to 35).

The introduction of the description has been adapted to the wording of amended Claim 1 and supplemented by a brief

summary of the relevant content of document D1 in order to meet the requirements of Rule 27(1)(c) and (d) EPC. In addition, the fact that the junction sustaining voltage can be enhanced by an increase in the thickness of the gate oxide layer (page 1, lines 18 to 21) has been more clearly acknowledged as having been found by the inventors.

These amendments do not introduce any subject-matter extending beyond the content of the application as originally filed.

3. Although there is no specific embodiment described in the specification of an integrated circuit device being actually coupled directly to an external voltage source as defined in present Claim 1, performing such direct coupling is well within the normal competence of the skilled person, who does not require any additional information therefor.

Accordingly, the present application also satisfies the requirement of Article 83 EPC that the invention be disclosed in a manner sufficiently clear and complete for it to be carried out by a person skilled in the art.

4. Novelty.

4.1 Document D1 discloses a semiconductor integrated circuit device as defined in the preamble of Claim 1, which comprises a first MIS FET (B) for forming an internal circuit for a device operating at a standard voltage of 5 volts and a second MIS FET (C) which is adapted to receive a voltage higher than the standard voltage, the second MIS FET (C) having a channel length greater than that of the first MIS FET and having a gate insulator thickness greater than that of the first MIS FET (B), (Figure 3; page 8, lines 23 to page 9, line 35).

The subject-matter of Claim 1 is distinguished from the device known from document D1 by the features of its characterising portion, according to which the second MIS FET forms an output stage circuit directly coupled to an external voltage source of 12 volts. In contrast therewith the second MIS FET (C) of the known device is part of a peripheral circuit of an EPROM and adapted to handle a "high voltage" of typically 25 volts for writing information into the memory cell.

4.2 Document EP-A-033 028 (D2) discloses a semiconductor integrated device which comprises a first MIS FET (MOS transistor) for forming an internal circuit and a second MIS FET having a channel length and a gate insulator thickness greater than that of the first MIS FET (Claim 7).

This device is distinguished from the subject-matter of present Claim 1 in that the second MIS FET forms a first-stage transistor of an input circuit instead of an output stage directly coupled to an external voltage source, and the document further fails to specify the voltages at which the respective MIS FETs operate.

4.3 There is no further document cited in the European search report, and the document:

"Feldeffekttransistoren", Heinz Beneking, Springer Verlag, Berlin - Heidelberg - New York, 1973, pages 66 and 67 (D3)

relied upon by the Examining Division in its communication dated 26 March 1986 only discloses occurrence of the punch-through effect in MOS FETs exhibiting short channel lengths.

4.4 The subject-matter of Claim 1 is therefore considered to be novel within the meaning of Article 54 EPC.

5. Inventive step.

5.1 Claim 1 being directed to a semiconductor integrated circuit device wherein the second MIS FET is directly coupled to an external voltage source of 12 volts, it actually defines the use of an integrated circuit device as set out in the preamble of the claim for directly controlling an electrical device driven by such voltage, as mentioned also in the description (page 1, second paragraph).

5.2 Whilst integrated circuits exhibiting the features of the preamble of Claim 1 are known already from document D1, in the Board's opinion the cited prior art neither discloses nor suggests the use of the second MIS FET, which exhibits increased channel length and gate insulator thickness, as an output stage directly coupled to an external voltage source of 12 volts, which is substantially lower than its drain breakdown voltage, as defined in the characterising portion of the claim, in order to overcome the so-called "punch-through" phenomenon and to benefit instead from a reduced drain current characteristic.

As a matter of fact, the general teaching a skilled person can reasonably be assumed to deduce from document D1 is only that those MIS FETs in an integrated circuit device which have to stand high voltages approaching junction breakdown voltage should exhibit increased channel length and gate insulator thickness to provide an increased breakdown voltage. Document 2 on the other hand addresses the quite different problem of reducing the variations in transistor threshold voltage V_{th} and transistor amplification factor ß of MOS FETs as a consequence of the

manufacturing process, which results in reduced noise margin for high and low levels of input signals applied thereto (page 1, second paragraph), and it teaches that these variations may be reduced by increasing the channel length and gate insulator thickness of the first-stage transistor of the input circuit.

None of these documents addresses the problem of achieving a reduction in the drain current of an output MIS FET directly coupled to an external source of voltage substantially below the breakdown voltage, nor even suggests that the junction sustaining voltage, which is far below the breakdown voltage, may be affected by a variation in thickness of the gate insulator layer.

Document D3 does not relate to an integrated circuit device comprising MIS FETs of different channel lengths and gate insulator thicknesses, neither does it contain any hint to the existence of an influence of such gate insulator thickness on the "punch-through" phenomenon referred to therein.

5.3 For these reasons, the subject-matter of Claim 1 is considered to involve an inventive step within the meaning of Article 56 EPC.

The same conclusion applies to the subject-matter of dependent Claim 2, which defines a particular embodiment of the invention set out in Claim 1.

6. Thus, the claims of the present application define patentable subject-matter within the meaning of Article 52(1) EPC, and they are accordingly allowable.

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent on the basis of the documents handed over by the Appellant during the oral proceedings on 7 July 1988.

The Registrar: The Chairman:

F. Klein K. Lederer