

Publication in the Official Journal  Yes / No

File Number: T 382/87 - 3.5.1

Application No.: 82 300 454.4

Publication No.: 0 057 111

Title of invention: Read only memory

Classification: G11C 17/00

DECISION  
of 3 July 1992

Applicant: General Instrument Corporation

Headword:

EPC Article 56

Keyword: "Inventive step (yes, after amendment)"

Headnote



Case Number : T 382/87 - 3.5.1

**D E C I S I O N**  
of the Technical Board of Appeal 3.5.1  
of 3 July 1992

**Appellant :** General Instrument Corporation  
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**Decision under appeal :** Decision of Examining Division 067 of the  
European Patent Office dated 27 February 1987  
refusing European patent application  
No. 82 300 454.4 pursuant to Article 97(1) EPC.

**Composition of the Board :**

**Chairman :** P.K.J. van den Berg  
**Members :** Y.J.F. van Henden  
C. Holtz

Summary of Facts and Submissions

- I. European patent application No. 82 300 454.4, filed on 28 January 1982, claiming the priority of the earlier application No. 229 717 of 28 January 1981 in the USA and published under No. 0 057 111, was refused by a decision of Examining Division 2.2.01.067 dated 27 February 1987.
- II. The reason given for the refusal was that, having regard to the prior art documents

- (D1) US-A-4 202 044,  
(D2) WO-B-80/01 119, and  
(D3) Electronique Industrielle, No. 7 (1 December 1982), page 22, article headed "Comment doubler leur capacité sans accroître leur surface",

the subject-matter of independent Claims 1 and 11 received on 15 October 1986 lacked an inventive step.

- III. On 23 April 1987, the Applicant lodged an appeal against that decision. The corresponding fee was paid on 24 April 1987 and the Statement of Grounds of Appeal was received on 3 July 1987.

Besides cancellation of the impugned decision and allowance of the claims on which said decision was based, the Appellant requested the appeal fee to be reimbursed but did not put forward any reason therefor.

- IV. On 12 December 1990, the Appellant submitted new Claims 1 to 3 and 5 to 8, and, on 26 October 1991, new Claims 4 and 9 to replace those previously on file.

Claims 1 and 3 are independent, the first one reading

"A read only memory comprising a plurality of field effect transistors (FETs) (26) interconnected in rows and columns in a matrix, each of said matrix FETs having one of at least three possible conditions, and input means for applying to a selected FET, an input signal for stimulating an output signal from said FET in accordance with the predetermined condition of said FET, the FET output signal, in operation of the memory, being applied to output means for producing a binary output in dependence upon the FET output signal, the matrix FETs (26) each having a gate region of substantially the same surface area and shape, and at least two of the possible conditions of each FET being determined by different gate threshold levels and a further possible condition being determined by a further different gate threshold level responsive to a further different input signal amplitude, or not being responsive to the input signal at all; characterised in that: reference FETs (36, 38, 40) each having a respective one of the different threshold voltages of the responsive matrix FETs are provided in each row of the matrix; the input means (28) is operable to apply to the matrix FETs of the row comprising the selected FET, during a predetermined read time interval, a ramp signal including the different threshold levels displaced in time from each other and from the beginning of the read time interval; the signal outputted by each reference FET is applied to a first input of a respective flip-flop (42, 44, 46); the signal outputted by the selected matrix FET is applied to a second input of each flip-flop; and the signals outputted by the flip-flops are applied to means (48) which, in dependence upon the flip-flops not changing their state or in dependence upon the time sequence of their changes of state, produces a binary output representative of the condition of the selected FET."

The pre-characterising part of Claim 3 is nearly identical to that of Claim 1, the only difference being that the parts of the draft reading "a further possible condition being determined by ..." in Claim 1 is replaced in Claim 3 by "a further possible one of which is determined by ...". The characterising part of Claim 3 reads

"characterised in that: reference FETs (36, 38, 40) each having a respective one of the different threshold voltages of the responsive matrix FETs are provided in each row of the matrix; the input means (78) is operable to apply a step voltage to the matrix FETs of the row comprising the selected FET; the current flowing through each reference FET is fed to a first input of a respective comparison circuit (82, 84, 86); the current flowing through the selected matrix FET is fed to a second input of each comparison circuit; and the signals outputted by the comparison circuits are applied to means (48) which, in dependence upon no coincidence being detected by said comparison circuits or in dependence upon the detected one, produces a binary output representative of the condition of the selected FET."

Claim 2 is appended to Claim 1, whereas Claims 4 to 9 are, directly or not, appended to any one of Claims 1 to 3.

V. The Appellant requests a European patent to be granted on the basis of the following documents:

Description : pages 1 to 3, 11 and 13 received on 26 October 1991 with letter of 23 October 1991; pages 5 and 6 received on 15 October 1986 with letter of 9 October 1986; page 4 received on 5 October 1989 with letter of 2 October 1989; pages 7 to 10, 12, 14 and 15 of the published patent application;

Claims : 1 to 3 and 5 to 8 submitted by telecopier on  
12 December 1990; 4 and 9 submitted on  
26 October 1991 with letter of  
23 October 1991;

Drawings : sheets 1/4 to 4/4 as initially filed,

with the following amendments requested or agreed to in  
his former submissions dated 9 October 1986,  
2 October 1989, 20 April 1990 and 12 December 1990:

- page 4, deletion of lines 5 and 6;
- page 5, replacement of "cell" by "matrix FET" in the  
first line and of "cells" by "gate regions" in  
line 27;
- page 7, deletion of the comma in the first line;
- page 8, lines 20, insertion of conjunction "if"  
between "or" and "transistor";
- page 9, addition of "s" at the end of "output" and  
"flip-flop" in lines 11 and 12;
- page 10, addition of "s" at the end of "state" in  
line 2; deletion of the first comma in line 3;  
replacement of "-0.2" by "-2.0" in line 7;  
replacement of "delayed circuit" by "delay circuit or  
device" in last but one line; replacement of  
reference number "46" by "40" at the end of the last  
line;
- page 12, replacement of text covering the lines 25 to  
27 by "to the first one previously set out except

that, in this embodiment, the outputs are of the comparison circuits 82, 84, 86 rather than of the flip-flops 42, 44, 46 as in the previous embodiment.";

- page 14, replacement of indefinite article "an" by "a modification of the" in line 6; replacement of the first semi-colon by a hyphen in lines 9, 10, 11; replacement of the sentence starting at line 26 by "In the embodiment described, three levels in an operating FET have been used.";
- page 15, line 18, correction of the spelling mistake in "metallization" and addition of "s" at the end of "region"; insertion of "ROM embodying the" between "the" and "present" in line 20; replacement of "doubles" by "enables" in line 20; insertion of "to be doubled" between "cell" and "would" in line 21;
- sheet 4/4 of the drawings, Figure 4, addition of reference number (78) relating to the step generator

and with the correction of minor clerical errors the Board still might detect.

#### Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is, therefore, admissible.
2. The amendments made to the application documents do not contravene Article 123(2) EPC and are, therefore, also admissible.

3. Novelty

3.1 In the Board's judgment, document (D1) reveals the closest prior art. This document pertains to a "read only memory" - see the title. Said memory "comprises a plurality of FETs (Q11, Q12, ..., Q14; Q21, ..., Q24; ...; Q41, ..., Q44) interconnected in bit lines (Q11, Q12, ...) (Q21, Q22, ...), ..., (Q41, Q42, ...) and word lines (Q11, Q21, ..., Q41), (Q12, Q22, ..., Q42), ..., (Q14, Q24, ..., Q44) in a matrix" - see Figure 2 and column 3, lines 18 to 27. During the manufacture of the ROM, each of the FET storage elements (Qij) in the array is selectively ion implanted in its channel region with one of four doses of conductivity enhancing dopant so as to achieve one of four predetermined threshold voltages -see column 3, lines 40 to 45. Therefore, in the terminology of the prior art parts of Claims 1 and 3 of the present application, "each of the matrix FETs has one of at least three possible conditions, at least two of which are determined by different gate threshold levels and a further possible one of which is determined by a further different gate threshold level responsive to a further different input signal amplitude". The dose of conductivity enhancing dopant being, among the parameters determining the threshold voltage of the FETs, the only one which may be varied during the manufacture of the ROM, it is appropriate to assume that the remaining such parameters are left unchanged and, therefore, are identical for all FETs in the matrix. It is well known that the dimensions of the gate regions are such remaining parameters. Therefore, it seems reasonable to assume that (D1) also discloses FET matrices with FETs having different gate threshold voltages in which all FETs have gate regions with the same dimensions, i.e., in the terminology of the prior art parts of Claims 1 and 3, "have substantially the same area and shape".

The ROM known from (D1) also comprises "input means (6, 22) for applying to a selected FET (Qij) an input signal for stimulating an output signal from said FET in accordance with the threshold voltage - i.e. the "condition" - of said FET, which output signal is applied to output means (12, 16) for producing a binary output in dependence upon the FET output signal" - see: Figures 1, 2; column 4, lines 9 to 33 and column 6, lines 30 to 39.

3.2 With respect to the FETs of the ROM matrix known from (D1) which do not have the highest threshold voltage, the "condition" of the FETs having said highest threshold voltage is, again using the terminology of the prior art parts of Claims 1 and 3, clearly "determined by a further different gate threshold level responsive to a further different input signal amplitude". It is furthermore stated in column 4 of (D1), lines 4 to 8, that the largest threshold voltage desired may be established by leaving a thick field insulator over the FET channel region. Therefore, in the Board's judgment, document (D1) also contemplates read-only memories in which particular FETs "are not responsive to the input signal at all" in the sense of the prior art parts of Claims 1 and 3. As a matter of fact, this may not be contested since, while operating a ROM matrix of the kind known from (D1) and comprising switchable FETs exclusively, the FETs of the matrix having the highest threshold level will anyway remain "not responsive at all" if the maximum voltage applied to the gates is lower than said highest threshold level.

3.3 Therefore, the Board takes the view that the features of the invention mentioned in the pre-characterising part of Claim 1 are known in combination from document (D1).

The same applies to Claim 3, since the difference in wording with respect to the pre-characterising part of Claim 1 has no substantial consequence.

3.4 With respect to the characterising parts of Claims 1 and 3, the following is to be noted:

In the arrangement known from (D1), each bit line (10) is connected to a "quaternary sense amplifier (12)" which comprises three FETs (T1, T2, T3) having respective threshold voltages ( $V_{T1}$ ,  $V_{T2}$ ,  $V_{T3}$ ), a common drain terminal and a common gate terminal to which the output signal of the bit line is applied - see: Figures 1 and 5; column 4, lines 58 to 60; column 5, lines 36 to 39. Reading is initiated by a clock pulse ( $\phi_2$ ) applied to a word line (6) and the output signal of the bit line has a voltage ( $V_{IN}$ ) which is the difference between the voltage ( $V_{DD}$ ) applied to the drains of the matrix FETs during operation and the threshold voltage of the selected FET array device ( $Q_{ij}$ ) - see column 4, lines 23 to 28. Despite the statement that the voltage magnitude of the clocking pulse is at least as large as ( $V_{DD}$ ) - see column 4, lines 17 to 23 - it thus appears that said clocking pulse does not play the same part as the step voltage which, according to Claim 3 of the patent application, is applied to the gates of reference FETs (36, 38, 40).

The sources of FETs (T1, T2, T3) are respectively tied to voltages ( $V_1$ ,  $V_2$ ,  $V_3$ ), with ( $V_1 > V_2 > V_3$ ) - see column 5, lines 38 to 41 and column 6, lines 40 to 51. Transistor (T1) thus remains off as long as ( $V_{IN} - V_1 < V_{T1}$ ), (T2) remains off as long as ( $V_{IN} - V_2 < V_{T2}$ ) and (T3) as long as ( $V_{IN} - V_3 < V_{T3}$ ) - see column 5, lines 42 to 46. According as to whether all FETs (T1, T2, T3) are off, only (T1) is on, only (T3) is off or all FETs (T1, T2, T3)

are on - which, in each case, is related to the "state" of the selected matrix FET - the output voltage ( $V_{OUT}$ ) of the sense amplifier (12) is ( $V_{DD}$ ), ( $V_{DD} - V_1$ ), ( $V_{DD} - V_2$ ) or ( $V_{DD} - V_3$ ), respectively. Stable states respectively corresponding to the quaternary levels (3,2,1,0) are thus given - see from column 5, line 42 to column 6, line 8.

Therefore, no reason why the threshold voltages ( $V_1$ ,  $V_2$ ,  $V_3$ ) of the FETs ( $T_1$ ,  $T_2$ ,  $T_3$ ) should respectively be equal to the second highest, second lowest and lowest threshold voltages of the matrix FETs, as mentioned in the characterising parts of Claims 1 and 3, can be perceived. As a matter of fact, the validity of this conclusion is confirmed by the numerical examples given in (D1) - see column 4, lines 36 to 39 and column 6, lines 48 to 51. Furthermore, in (D1), no response of the selected matrix FET is compared with a corresponding response of one of the FETs ( $T_1$ ,  $T_2$ ,  $T_3$ ). The latter, therefore, do not constitute "reference FETs" within the meaning of the patent application and thus, in (D1), no comparison circuits are provided, which deliver output signals to be applied to means producing a binary output representative of the "condition" of the selected FET.

In the Board's judgment, therefore, since none of the features of the characterising part of Claim 3 is known from (D1), the subject-matter of independent Claim 3 is novel with respect to this prior art. This claim is correctly delimited with respect to this prior art.

- 3.5 In a ROM according to Claim 1, the flip-flops connected to reference FETs having a threshold voltage lower than or equal to the threshold voltage of the selected FET change their state at the time when the voltage of the ramp signal becomes equal to said threshold voltage of the selected FET, at least if the latter is responsive. Each flip-flop connected to a reference FET having a higher

threshold voltage than the selected FET, if any, changes its state when the voltage of the ramp signal becomes equal to the threshold voltage of said reference FET, i.e. later. A ROM according to Claim 1 is thus provided with means suitable for detecting, if such event actually occurs, the coincidence of times at which the selected FET and one of the reference FETs become conductive. The ROM known from (D1) is, however, not provided with such means, nor with means suitable for applying a ramp signal to the gate of any FET.

In the Board's judgment, therefore, the subject-matter of independent Claim 1 is novel with respect to the prior art which can be derived from document (D1) in that it is distinguished from this document by the characterising part, so that independent Claim 1 too is correctly delimited with respect to this prior art.

3.6 According to (D2), the condition of a matrix FET is determined by applying a voltage ( $V_{row}$ ) to the gates of the FETs belonging to a selected line and by comparing the output voltage of one of these FETs to reference voltages ( $V_{12}$ ,  $V_{23}$ ,  $V_{34}$ ) comprised within the adjacent intervals limited by the respective output voltages ( $V_1$ ,  $V_2$ ,  $V_3$ ,  $V_4$ ) of the four different kinds of matrix FETs - see from page 7, line 20 to page 8, line 13. Nevertheless, neither the means generating the reference voltages nor the constitution of the sense amplifiers used for comparing said reference voltages with the output voltage of a selected FET are disclosed. None of the features mentioned in the characterising part of Claim 1 or 3, therefore, may be considered as explicitly or implicitly disclosed in (D2).

Therefore, in the Board's judgment, the state of the art disclosed in document (D2) does not come closer to the

subject-matter of independent Claims 1 and 3 than does the one known from (D1).

4. Inventive step

4.1 Documents (D1) and (D2) relate to ROMs comprising FETs interconnected in rows and columns in a matrix and, in order to identify the threshold voltage of a selected FET among four possible values, propose to compare the output voltage of said selected FET under given operating conditions with appropriate reference voltages, the parameters featuring the components of the comparison circuits being chosen such as to preclude coincidence of the voltages to be compared. These documents, therefore, lead the skilled person away from the idea of discriminating on the basis of coincidence between compared values, and actually the more so as (D1) explicitly mentions the problem of tolerances - see column 5, lines 11 to 14 and column 6, lines 17 to 20 - whereas (D2) recommends to choose reference voltages which are "an average of the three pairs of adjacent FET output voltages" - see the sentence bridging pages 7 and 8. It is thus beyond doubt that the skilled person following routine would declare himself satisfied with one of the solutions disclosed in (D1) and (D2).

Now, even if the idea of discriminating on the basis of coincidence between a parameter featuring the response of a sensed FET and a physical parameter of the same nature had been suggested to the skilled person, an initiative would nevertheless still have been required from him to envisage the use of reference FETs having each a respective one of the different threshold voltages of the responsive matrix FETs. For said skilled person starting from the state of the art as disclosed in (D1) and (D2), the application of the idea of discriminating on the basis of coincidence would clearly only consist in comparing a

FET output voltage with reference voltages so as to detect coincidence instead of superiority or inferiority. Thus, no need for designing any new circuit would be felt since it would be enough to adapt accordingly the sources already in use in known devices for providing the reference voltages, or to pick up such reference voltages between connections to resistive potentiometers.

Therefore, having regard to Claim 3, the exercise of inventive ingenuity was needed to provide each row of the matrix with reference FETs each having a respective one of the different threshold voltages of the responsive matrix FETs, to provide means for applying a step voltage to the gate of a selected FET and to the gates of the reference FETs belonging to the same row, and to provide means suitable for detecting whether one of the currents flowing through the reference FETs has the same intensity as the current flowing through the selected FET and, if such is the case, which one. Likewise, having regard to Claim 1, the exercise of inventive ingenuity was also needed to provide each row of the matrix with reference FETs each having a respective one of the different threshold voltages of the responsive matrix FETs, to provide means for applying a ramp voltage to the gate of a selected FET and to the gates of the reference FETs belonging to the same row, and to provide means suitable for detecting whether one of the reference FETs becomes conductive at the same time as the selected FET and, if such is the case, which one.

4.2 Therefore, the subject-matter of independent Claims 1 and 3 involve an inventive step.

5. In its communication dated 12 April 1989, the Board had indicated that the subject-matter of the then valid Claim 1 and the embodiment of Figure 4 of the application were not so linked as to form a general inventive concept

and that, if the valid claims were not amended to take account of this, Figure 4 and its description would have to be deleted. After amendments, present Claim 1 now covers the embodiment of Figure 2 and present Claim 3 covers that of Figure 4 of the application, as had been suggested in the said communication. The foregoing reason 4 of this decision shows that the inventions as defined by these claims are indeed so linked as to form a single general inventive concept and therefore meet the requirements pursuant to Article 82 EPC.

6. Independent Claims 1 and 3 are allowable - Article 52(1) EPC in relation with Article 56.

The same applies to the dependent Claims 2 and 4 to 9.

7. The file of the first instance does not reveal any irregularities. Therefore, and since the Appellant did not give any reason in support of his request for a refund of the appeal fee, the latter request has to be rejected.

#### Order

For these reasons, it is decided that:

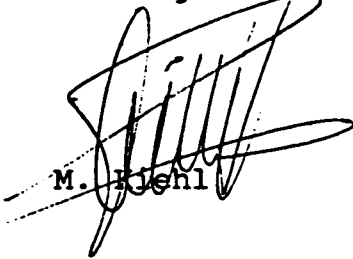
1. The decision under appeal is set aside.
2. The case is remitted to the first instance with the order to grant a European patent on the basis of the documents cited under numeral V of Summary of Facts and Submissions, with the amendments listed there and the following additional amendments:
  - deletion of the "t" preceding "input" in line 29 of the new page 2;

- replacement of "difference" by "different" in line 15  
of the new page 3.

3. The request for a refund of the appeal fee is rejected.

The Registrar:

The Chairman:



M. Hohl



P.K.J. van den Berg

