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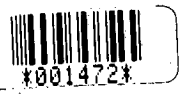

Aktenzeichen / Case Number / N° du recours : T 407/87 - 3.4.1

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Bezeichnung der Erfindung:
Title of invention:
Titre de l'invention : Semiconductor device having first and second electrodes and method of producing the same

Klassifikation / Classification / Classement : H01L 29/46, H01L 21/285

## ENTSCHEIDUNG / DECISION

vom / of / du 24 January 1989

Anmelder / Applicant / Demandeur : Kabushiki Kaisha Toshiba

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Article 56

Schlagwort / Keyword / Mot clé : Inventive step (yes)

**Leitsatz / Headnote / Sommaire**

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Case Number : T 407/87 - 3.4.1

# D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 24 January 1989

Appellant : Kabushiki Kaisha Toshiba
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Representative Lehn, Werner, Dipl.-Ing.
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Decision under appeal : Decision of Examining Division 048 of the European Patent Office dated 25 March 1987 refusing European patent application No. 84 105 669.0 pursuant to Article 97(1) EPC

Composition of the Board :

Chairman : K. Lederer
Members : J. Roscoe
G.D. Paterson

## Summary of Facts and Submissions

I. European patent application No. 84 105 669.0 (publication number 0 127 089) was refused by a decision of the Examining Division.

II. The reason given for the refusal was that the subject-matter of the effective single claim as filed on 25 March 1987 lacked an inventive step within the meaning of Article 56 EPC, having regard to the disclosure of documents US-A-3 686 698 (D1) and US-A-3 434 828 (D5). In particular, the claimed device was considered to be distinguished from the semiconductor device disclosed in document D5 only by the replacement of the Au-Sb gold alloy layer forming the known back surface electrode by an Au-Ge-Sb layer, which was obvious from document D5, and by the specification of thickness ranges for the electrode layers which were conventional in the art.

The Examining Division further stated in the decision that it had serious doubts whether the single claim and the disclosure of the invention respectively met the requirements of Articles 84 and 83 EPC since the claim embraced any semiconductor material of any conductivity type, and that, in its opinion, this deficiency could not be rectified without infringing Article 123(2) EPC since the application documents as originally filed did not disclose any particular semiconductor substrate.

III. The Appellant lodged an appeal against the decision.

IV. Oral proceedings were held on 24 January 1989, at the end of which the Appellant requested that the decision be set aside and that a patent be granted on the basis of Claims 1 to 4 as filed during the oral proceedings, of which independent Claims 1 and 3 read as follows:

"1. A semiconductor device including:

a silicon substrate (20) provided with a plurality of N-type semiconductor regions (21, 23) and an insulation film (26) formed on the front surface;

a front surface electrode (28) connected to a prescribed semiconductor region (25) via an opening made in the insulation film (26); and

a back surface electrode (29, 30) consisting of a gold alloy layer (29) formed on the back surface of the substrate (20) and a silver layer (30) formed on the gold alloy layer, the gold alloy layer being formed by vapour deposition,

c h a r a c t e r i z e d i n t h a t

said gold alloy layer (29) is an Au-Ge alloy layer formed by vapour deposition of Au and Ge directly onto the silicon substrate to have a thickness of 50-500 nm and

said silver layer (30) has a thickness of 1.5-3.0 $\mu$m.

3. A method of producing a semiconductor device, comprising the steps of:

forming a front surface electrode connected to a prescribed semiconductor region of a silicon substrate, provided with a plurality of N-type semiconductor regions, via an opening made in an insulation film formed on the substrate surface;

polishing the back side of the substrate to a prescribed extent;

depositing an Au-Ge alloy layer directly onto the substrate by vapour deposition, said layer having a thickness of 50-500 nm and providing a part of the back surface electrode on the polished back surface of the substrate; and

forming a silver layer having a thickness of 1.5-3.0 $\mu$m and providing a part of the back surface electrode on the Au-Ge alloy layer."

Claims 2 and 4 are appended to independent Claims 1 and 3, respectively.

V. In support of the allowability of his request, the Appellant essentially submitted that, in contrast with the conventional techniques involving specific heat treatment to form an alloy such as a nickel silicide or an alloy of gold and silicon at the interface between substrate and back electrode of a semiconductor device, the present invention was based on the recognition that satisfactory adhesivity of the back surface electrode could be achieved simply by vapour depositing an alloy of gold and germanium on the semiconductor substrate.

The capacity of germanium to improve the bonding strength of an electrode layer made of an Au-Ge alloy when vapour deposited on a semiconductor substrate, which was not apparent when using a different deposition technique, was not predictable from the prior art, which even led away from contemplating the use of an Au-Ge alloy layer on a silicon substrate, as was now specifically set out in the claims.

With regard to the admissibility under Article 123(2) EPC of the additional limitation introduced into the claims to specify that the semiconductor substrate was made of silicon, the Appellant submitted that adequate disclosure of this specific substrate material resulted from the indication in the description as originally filed that insulation film 24 of the device described with reference to Figure 6, which was formed by thermal oxidation of the surface of the semiconductor substrate (page 6, lines 20 to 25), consisted, for example, of silicon dioxide (page 5, lines 10 to 13).

Finally, since determining which specific alloy compositions and operating parameters of the vapour deposition process allowed achievement of adequate electrode adhesivity did not require more than the performance of simple routine tests, the present claims, which did not comprise any limitation in this respect, were properly supported by the description as required under Article 84 EPC, even in the absence of any detailed example or other information specifying adequate ranges for the alloy composition and evaporation conditions.

VI. At the end of the oral proceedings the decision was announced that the patent would be granted on the basis of the Appellant's request.

**Reasons for the Decision**

1. The appeal is admissible.

2. There is no objection under Article 123(2) EPC to the present application documents, since they are adequately supported by the application documents as originally filed.

In particular, present independent Claims 1 and 3 comprise in substance the features of original Claims 1 and 4, respectively, together with additional features relating to the nature, thickness and deposition process of the gold alloy layer as set out in original Claims 2, 3 and 5, to the type of the plurality of semiconductor regions provided on the substrate and to the thickness of the silver layer as respectively disclosed in the original description page 5, lines 1 to 5 and page 6, lines 5 to 7, and to the nature of the semiconductor substrate, which is now specified to be made of silicon. The latter feature is implicitly disclosed in the original application documents by reference to the nature and formation method of insulating film 24, which is said to consist, for example, of silicon dioxide and to be formed by thermal oxidation of the surface of the semiconductor substrate (page 5, lines 10 to 13 and page 6, lines 20 to 25). These statements both relate to the sole embodiment of the invention actually disclosed in the application and illustrated in Figures 4 to 13, and they are not therefore independent from each other as was assumed by the Examining Division. When considered in combination, they clearly designate silicon, which is the sole semiconductor material thermally oxidizable into silicon dioxide, as an example of a suitable material for the semiconductor substrate.

3. The Board has carefully considered whether the requirement of Article 83 EPC is met in this case: this question was the subject of considerable discussion at the oral hearing. In particular, Rule 27(1) EPC specifically requires that the description of a European patent application shall "(f) describe in detail at least one way of carrying out the invention claimed using examples where appropriate ... ". The description of the present application is conspicuous by the absence of any specific example setting out a way of carrying out the claimed invention, and of any specific details of the manner in which the vapour deposition of the

alloy should be performed, especially with regard to the amount of germanium to be used and the temperature of the vapour deposition process. But the requirement in Rule 27(i)(f) quoted above that there should be examples where appropriate must be interpreted in the sense that examples should be included when appropriate for the purpose of satisfying the requirement of sufficiency in Article 83 EPC.

In the present case, there is no documentary evidence on file casting doubts on Appellant's submission that assessing which alloy compositions and operating conditions actually lead to formation of an effective back surface electrode calls only for routine investigation of the performance of alloy layers of different compositions as vapour deposited under conventional conditions onto the semiconductor substrate. The experimental work required to determine these parameters also appears to be reasonably limited in extent, because silicon is the sole substrate material to be tested, and, in view of the designation, throughout the description and claims of the Au-Ge alloy layer as a "gold alloy" layer, compositions including more germanium than gold need not be investigated either.

For these reasons, the Board is satisfied on the evidence before it that the present case is exceptional in that, in the present circumstances, failure of the description to include any detailed example or other information disclosing specific ranges of the alloy composition or of the operating conditions of the vapour deposition process does not render the disclosure of the invention insufficient; and considers that the claims, though not explicitly limited to any specific ranges either, but which in the light of the description must nevertheless be considered to cover only embodiments which are effective to achieve high electrical conductivity and high adhesivity to the substrate (see sentence bridging pages 5 and 6 of the

description), are adequately supported by the description. In the Board's view, the present application documents therefore meet the substantive requirements of Articles 83 and 84 EPC.

4. Novelty.

4.1 Document D1 discloses a semiconductor device including a silicon substrate (1) provided with a plurality of N-type semiconductor regions (1, 2) and an insulation film (4) formed on the front surface, a front surface electrode (6, 7) connected to a prescribed semiconductor region (3) via an opening made in the insulation film (4), and a back surface electrode (9, 10) consisting of a gold alloy layer (9) formed on the back surface of the substrate (1) and a silver layer (10) formed on the gold alloy layer, the gold alloy layer being formed by vapour deposition, as set out in the preamble of present Claim 1. (Figure 4; column 2, lines 57 to 64 in connection with column 1, line 51 to column 2, line 9).

The subject-matter of Claim 1 is distinguished from this known device in that the gold alloy layer is an Au-Ge alloy layer which may include antimony as well (see present Claim 2) instead of an alloy of gold and antimony only, and in that the thicknesses of the gold alloy and silver layers, which are not specified in document D1 lie in the ranges set out in the characterising portion of the claim.

4.2 Document DE-A-2 643 147 (D3) discloses a semiconductor device including a silicon substrate provided with a plurality of N-type semiconductor regions (11, 12) and an insulation film (16) formed on the front surface, a front surface electrode (15, 17) connected to a prescribed semiconductor region (13) via an opening made in the insulation film, and a back surface electrode comprising an Au-Ge alloy layer (21) formed by vapour deposition on a

silver layer 20. The thicknesses of the Au-Ge alloy and silver layers are comprised in the ranges between 250 and 370 nm ("10 bis 15 Mikrozoll") and 0.75 and 1.75 $\mu$m ("30 bis 70 Mikrozoll") respectively, which partially overlap the corresponding ranges specified in present Claim 1. (D3; Figure 1 and page 3, line 11 to page 6, line 19 of the description as originally numbered).

In contrast with the claimed back surface electrode structure, the Au-Ge alloy layer (21) of the back surface electrode known from document D3 is neither formed directly onto the silicon substrate nor provided with an overlying silver layer, but is formed on a silver layer (20) which itself is formed on a nickel layer (18). The nickel layer (18) is first deposited on the silicon substrate (11) and then sintered to form a nickel silicide region at the interface between the substrate and the back surface electrode.

4.3 Document D5 relates to gold alloys for soldering leads to a semiconductor body, in particular for the manufacture of transistor devices. A gold alloy essentially comprising gold and germanium is disclosed.

This Ge-Au alloy is neither vapour deposited nor used for forming back surface electrodes of silicon semiconductor devices.

4.4 The remaining cited documents do not come closer to the subject-matter of Claim 1.

4.5 For these reasons, the subject-matter of Claim 1 is considered to be novel within the meaning of Article 54 EPC.

5. Inventive step.

5.1 The technical problem to which the device defined in Claim 1 achieves a solution as objectively assessed in view of the nearest prior art, which in the Board's view is disclosed in document D1, is to provide an alternative semiconductor device structure providing high electrical conductivity and high adhesivity of the back surface electrode formed on the silicon substrate while simultaneously avoiding the drawbacks of forming a sintered nickel layer as required in the conventional alternative referred to in the introductory portion of the description of the present application (sentence briding pages 5 and 6) or disclosed in document D3.

This problem is solved in accordance with Claim 1 essentially by the use of an Au-Ge alloy to form the vapour deposited gold alloy layer on the silicon substrate.

5.2 The ability of an Au-Ge alloy to form an effective contact electrode when directly evaporated onto a silicon semiconductor substrate was not, in the Board's view, predictable from the available prior art.

Document D5 in particular recommends use of an Au-Ge alloy as a contacting material only for germanium transistors to overcome the drawbacks of the higher melting point of pure gold and its capacity to absorb germanium from the germanium transistor bars, which are thus rendered thin and brittle (abstract; column 5, lines 23 to 32), and it clearly leads away from the claimed solution by teaching that silicon should "obviously" replace germanium in the alloy for use with silicon transistors (column 7, lines 4 to 10).

Document D1 stresses the necessity of forming an eutectic alloy of gold and of the semiconductor material on which the gold alloy is vapour deposited (abstract), which also leads away from the idea of incorporating into the

deposited gold alloy layer a semiconductor material different from that of the substrate.

Document D3, which is the sole document on file to disclose a back surface electrode of a silicon semiconductor device comprising a layer of an Au-Ge alloy, does not provide any hint at depositing such layer directly onto the silicon surface either, for the Au-Ge alloy described in the document is an outer layer which is separated from the semiconductor substrate material by intermediate layers of nickel silicide and silver, and which is used for the different purpose of causing metallurgical interaction with the particular Dumet material of the connecting studs (31, 32) (paragraph bridging pages 6 and 7 of the description). The interface between the back surface electrode and the silicon substrate is constituted for its part by a layer of nickel silicide formed by sintering, which is just what the present invention aims to avoid.

Accordingly, the skilled person a priori had no reasonable ground to provide a layer of an Au-Ge alloy directly onto the surface of the silicon substrate of the device of document D1, and for this reason alone, the subject-matter of independent Claim 1 is considered to involve an inventive step within the meaning of Article 56 EPC.

The same reasoning applies to the method of independent Claim 3, since it also involves providing an Au-Ge alloy layer by direct deposition on a silicon substrate to form the substrate-adjacent part of a back surface electrode.

6. For the above reasons, independent Claims 1 and 3 are allowable under Article 52 EPc. Dependent Claims 2 and 4 are also allowable by virtue of their dependence on allowable independent claims.

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent on the basis of the following documents:

Description: pages 1, 4, 4a and 6 handed over at the oral proceedings of 24 January 1989
pages 2, 3 and 4b filed on 29 September 1987
pages 5, 7 and 8 as originally filed.

Claims: 1 to 4 handed over at the oral proceedings of 24 January 1989.

Drawings: page 1/4 to 4/4 as originally filed.

The Registrar: The Chairman:

F. Klein K. Lederer