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Bezeichnung der Erfindung: Frequency modulation transmitter
Title of invention:
Titre de l'invention :

Klassifikation / Classification / Classement : H03C 3/09

ENTSCHEIDUNG / DECISION

vom / of / du 11 October 1988

Anmelder / Applicant / Demandeur : Nippon Electric Co., Ltd.

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Article 56

Schlagwort / Keyword / Mot clé : Inventive step (no)

Leitsatz / Headnote / Sommaire

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number : T 424/87 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal
of 11 October 1988

Appellant : NIPPON ELECTRIC CO.,LTD.
33-1, Shiba Gochome, Minato-ku
Tokyo, 108 (JP)

Representative : Bohnenberger, Johannes
Meissner, Bolte & Partner
Widenmayerstrasse 48 Postfach 86 06 24
D-8000 München 86 (DE)

Decision under appeal : Decision of Examining Division 056 of the European Patent Office dated 23 June 1987 refusing European patent application No. 82 111 634.0 pursuant to Article 97(1) EPC

Composition of the Board :

Chairman : P.K.J. van den Berg
Members : W.P.H. Riewald
R.E. Persson

Summary of Facts and Submissions

I. European patent application No. 82 111 634.0 was filed on 15 December 1982, claiming priority from a Japanese application of 17 December 1981.

The application was refused by a decision of the Examining Division dated 23 June 1987.

The reason given for the refusal was that the subject-matter of the claims lacked an inventive step having regard to the following document:

D1: GB-A-2 031 676

II. The Appellant filed a notice of appeal and paid the appeal fee on 3 September 1987.

A statement of the grounds of appeal was filed together with a new Claim 1 on 3 November 1987.

In a communication, accompanying summons for oral proceedings, the Rapporteur made additional reference to the following documents:

D2: "encyclopedia of instrumentation and control", McGraw-Hill, Inc. 1971, pages 647 and 648;

D3: "Semiconductor Data Library" Vol. 5/Series B, Motorola Inc., 1976, pages 5-124 to 5-129

and expressed the provisional opinion that the subject-matter of the claims lacked an inventive step.

A new Claim 1 and amendments to the description were filed on 27 September 1988.

Oral Proceedings were held on 11 October 1988.

III. The Appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of Claim 1 received on 27 September 1988 and Claim 2, filed on 5 May 1986 by way of the main request and as an auxiliary request the combination of said two claims into a single claim.

IV. Claims 1 and 2 read as follows:

"1. A frequency modulation transmitter having M (M is positive integer) sub-frequency bands within a transmission frequency band in use comprising:

a loop circuit including a voltage controlled oscillator (1), a frequency divider (2) for frequency dividing an output signal of said voltage controlled oscillator (1), comparator for comparing an output signal of said frequency divider (2) with a reference frequency signal (f_R) and a lowpass filter (7) for filtering an error signal output from said comparator to output the filtered signal to said voltage controlled oscillator, said loop circuit inputting a modulation signal to output a frequency modulated signal;

a channel controller (3) for supplying a channel designation signal to said frequency divider (2) to set a frequency division ratio of said frequency divider (2) and outputting a first control signal representing the designated channel;

an input section (11, 12, 13) supplied with an input signal for amplifying and filtering the input signal;

a transmitter section (33) for transmitting the frequency modulated signal output from said loop circuit; and

level setting means (14, 15, 16, 17, 18, 19, 21, 22), responsive to the first control signal from said channel controller (3), for inputting the output signal of said input section (11, 12, 13) to output the modulation signal having a level corresponding to the channel designated by said channel controller (3) to said loop circuit;
c h a r a c t e r i z e d i n t h a t
said level setting means comprising:

M resistors (14, 15, 16) having one terminal thereof commonly connected to an output terminal of said input section, the other terminals commonly connected to the ground and output terminals adjustably provided between the one and the other terminals respectively;

N switches (17, 18, 19) connecting and disconnecting between the output terminals of said resistors and an input terminal of said loop circuit, respectively, under the control of a second signal; and

a decoder means (21, 22) for decoding the first control signal received from said channel controller to output the second control signal to said N switches so that only one corresponding to the designated channel of said N switches turns on.

2. A frequency modulation transmitter according to Claim 1 wherein the level setting means is constituted of the

plurality of adjustable means and a one-chip IC analog multiplexer which includes a plurality of input terminals, an output terminal, a control terminal, a level converter having input terminal connected with the control terminal, a decoder circuit having an input terminal connected with the output terminal of the level converter, the decoder circuit having a plurality of output terminals corresponding to the codes, respectively, a plurality of analog switches, each having an input terminal connected to the corresponding input terminal, an output terminal connected with the output terminal of the analog multiplexer, and control terminal connected with the corresponding output terminal of the decoder circuit, the plurality of input terminals, the output terminal and the control terminal of the analog multiplexer being connected to the adjustable means, the voltage oscillator and the channel controller, respectively."

V. The Appellant argues essentially as follows:

Claim 1 starts in its precharacterising portion from a frequency modulation transmitter as disclosed in Figure 1 of D1. In contrast to the characterising features of Claim 1, the level setting means are only disclosed as comprising a store (14) and a tracking amplifier (9). Resistors connected to the circuit by switches which are controlled by decoder means are not disclosed in connection with this prior art embodiment.

Switch controlled resistors as level setting elements are only known from the embodiment described in connection with Figure 2 of D1, this embodiment not being a further development of Figure 1 but an embodiment of a different type since it makes use of a "variable oscillator" instead of a "phase lock loop" with a controllable "frequency

divider". Furthermore, the realisation with a store (10) constituted as a read-only memory according to page 3, lines 82 to 90 of D1 is clearly distinguished from the main concept of D1 which concentrates on automatic means for a calibration of the level setting means in dependence on a measurement of the frequency modulation sensitivity of the voltage controlled oscillator. With a read-only memory as store, an adaption of the level setting means to a different oscillator would, for instance, require a replacement of the whole read only memory. This is more complicated than an adjustment of the resistors (14, 15, 16) in the claimed transmitter circuit.

Starting from Figure 2 of D1, the Appellant sees mainly three steps for arriving at the claimed subject-matter:

- Replacement of the store (10) in D1, which may be a read-only memory, by a decoder which is a means that is less complicated and acts faster since a read-only memory requires a clock control whereas a decoder directly outputs a decoded signal in response to the input signal.

- Replacement of a "variable oscillator" by a "phase lock loop".

- Calibration of the level setting means not by reprogramming of the store with the effect of differently switching on fixed resistance values but by adjusting the resistance values and use of a fixed decoder.

Finally, an analog multiplexer as specified in Claim 2 has not yet been used for a transmitter circuit of the present type.

Reasons for the Decision

1. The appeal is admissible.

2. Novelty

A frequency modulation transmitter with the essential features of the precharacterising portion of Claim 1 is known from Figure 1 of D1:

A phase lock loop circuit 2 includes a voltage controlled oscillator 1, a frequency divider 3 for frequency dividing an output signal of said voltage controlled oscillator, a comparator (phase detector) 4 for comparing an output signal of said frequency divider with a reference frequency signal (input 7, page 1, lines 58-61) and a lowpass filter 5 outputting the filtered signal through an adder 6 to the voltage controlled oscillator 1.

The adder 6 receives, in addition, a modulation signal (from terminal 17) so that the loop circuit outputs at terminal 8 of the voltage controlled oscillator 1 a frequency modulated signal.

A channel controller (frequency selector) 13 supplies a control signal to the frequency divider 3 to set a frequency division ratio representing a designated channel of the transmission.

Responsive to a further control signal of the channel controller is a tracking amplifier 9. This tracking amplifier sets the level of the modulation signal in correspondence with the channel designated by the channel controller (frequency selector) 13. A store 14, which may be constituted as a read-only memory (page 2, lines 42 to 50) serves as means for transforming the control signal received from the channel controller to a level setting

signal for the tracking amplifier. That read-only memory performs, therefore, already the function of a decoder so that this feature from the last part of the characterising part of Claim 1 is not novel.

An input section for the modulation signal and a transmitter section for the frequency modulated signal, specified in the precharacterising part of Claim 1 are not explicitly mentioned in D1. These elements are, however, self-evident if a frequency modulated signal is to be generated and transmitted.

What remains novel in Claim 1 against the closest prior art represented by Figure 1 of D1 is the realisation of the level setting means in the form of a switch controlled resistor arrangement as specified in the characterising part of Claim 1.

3. Inventive step.

3.1 In contrast to the Appellant's submission that the three embodiments disclosed in D1 are so different that a combination of features from Figures 1 and 2 is not immediately obvious, the Board is satisfied that the combinations to be considered in the present case suggest themselves from the said document.

The reader of D1 understands from page 1, lines 77 to 80 that the amplifier 9 is provided for modifying the gain of the frequency modulation signal as a function of a selected carrier frequency value. Reading further, he learns from page 2, line 109 to page 3, line 15 that the amplifier arrangement 5, 7, 8 of Figure 2 serves exactly the same purpose as the tracking amplifier 9 of Figure 1 at the input of the modulation signal. Therefore, the suggestion of Figure 2 to use switch controlled resistors as level

determining elements in various modifications (page 3, lines 42 to 58) is readily applicable also to the embodiment of Figure 1. Likewise, the omission of any details in Figure 2 concerning the variability of the variable oscillator 1, whose function in respect of creating a variable frequency modulated signal is the same as in Figure 1, readily conveys the idea that a possible embodiment of Figure 2 might comprise the phase lock loop with controllable frequency divider already disclosed in Figure 1.

3.2 The Board is, therefore, satisfied that the use of resistors controlled by switches in response to signals from the channel controller via decoder means is readily derivable from D1.

With this knowledge of the prior art, it is only a workshop modification to use, instead of series resistances as suggested in D1 (page 3, lines 42 to 58), resistance potentiometers within the signal path of the modulation signal. The resistances must be given the appropriate resistance values necessary to achieve the different modulation levels for the selected channels. It is, therefore, only a matter of routine to use adjustable resistances if, in practice, readjustment of the transmitter has to be envisaged for any reasons. The fact that this possibility is not mentioned in D1 is obviously due to the specific intention of this prior art to perform an automatic calibration which is easier to achieve by calibrating the store. If automatic calibration is not envisaged, which is the prior art from which D1 starts (page 1, lines 6 to 24), the skilled person will readily envisage calibration at any of the level defining elements of the modulation circuit.

3.3 Thus, the subject-matter of Claim 1, according to the main request, is not considered to involve an inventive step within the meaning of Article 56 EPC and Claim 1 is, therefore, not allowable under Article 52(1) EPC.

3.4 The same applies to the combination of Claims 1 and 2 according to the auxiliary request, since Claim 2 specifies only features of a well known analog multiplexer (D3, see in particular Figure 2 and the truth table) which is used as the decoder means.

The Appellant argues that the store 10 of Figure 2 of D1 in the form of a "read-only memory" (as suggested on page 3, lines 82 to 90) is a means to be distinguished from a "decoder". However, what is important is that the known store 10 performs the translation from an input signal (outputted from the frequency selector 3) into an output signal for switching contacts (in the resistor network 8). Such a switch control is exactly the function of the so-called analog multiplexer as disclosed in D3. There is no prejudice which could prevent the skilled man from substituting such a "decoder" for the read-only memory-controlled switch arrangement of D1, Figure 2.

Order

For these reasons, it is decided:

The appeal is dismissed.

The Registrar: The Chairman:

S. Fabiani P.K.J. Van den Berg