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Anmeldenummer / Filing No / N° de la demande : 81 305 914.4

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Bezeichnung der Erfindung: Output buffer circuit

Title of invention:

Titre de l'invention :

Klassifikation / Classification / Classement : G11C 17/00

ENTSCHEIDUNG / DECISION

vom / of / du 31 January 1989

Anmelder / Applicant / Demandeur : Fujitsu Limited

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Art. 56

Schlagwort / Keyword / Mot clé : "Inventive step (denied) - use of equivalent control criterion - extended effect is unsurprising logical consequence"

Leitsatz / Headnote / Sommaire

Europäisches
Patentamt

European Patent
Office

Office européen
des brevets

Beschwerdekammer

Boards of Appeal

Chambres de recours

Case Number : T 64/88 - 3.5.1



D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 31 January 1989

Appellant : Fujitsu Limited
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Decision under appeal : Decision of Examining Division 067 of the European Patent Office given on 23 March 1987 and notified on 26 August 1987 refusing European patent application No. 81 305 914.4 pursuant to Article 97(1) EPC

Composition of the Board :

Chairman : P.K.J. van den Berg

Members : W.B. Oettinger

F. Benussi

Summary of Facts and Submissions

- I. European patent application No. 81 305 914.4, filed on 17 December 1981 claiming a priority of 25 December 1980 and published under No. 55 551, was refused in oral proceedings held on 23 March 1987 by Examining Division 2.2.01.067.

- II. The reason for the refusal, given in a written decision dated 26 August 1987, was that in view of the prior art, the subject-matter of Claim 1 filed on 23 March 1987 did not involve an inventive step and that the same applied to the combined features of Claim 1 and Claims 2, 3, 4 and 9 filed on 3 December 1986, constituting the Appellant's subsidiary request.

As prior art, the following documents were considered:

- (D1) Patent Abstracts of Japan, volume 2 No. 42, 20 March 1978, page 495 E 78 (JP-Kokai-53-85 26)

- (D2) IEEE Journal of Solid State Circuits, volume SC-5 No. 5, October 1970, pages 196 to 202

- (D3a) The Semi-conductor Memory Book (Intel), J. Wiley & Sons 1978, pages 273 to 274

- (D3b) ditto pages 309 to 314

More particularly, the Examining Division concluded that a PROM device with an output buffer circuit as claimed in Claim 1 was rendered obvious by D3 and D2, in particular the latter, and that, on the basis of the same prior art, the dependent claims whose combination constituted the

subsidiary request did not add anything inventive to Claim 1.

- III. On 22 October 1987, the Applicant appealed against this decision, requesting its cancellation, and paid the appropriate fee.

He filed a Statement of Grounds of Appeal on 5 January 1988, accompanied, inter alia, by a new Claim 1 and contesting in particular the Examining Division's interpretation of D2.

- IV. In response to a communication from the Board, indicating, for instance, a lack of clarity in Claim 1 and drawing the Appellant's attention particularly to D3b, the Appellant filed a complete set of new application documents on 20 December 1988.

The independent claim reads as follows:

"1. A PROM device, in which a writing operation involves an increase in a power source voltage applied to the device, comprising an output buffer circuit capable of taking any of three output states, high level, low level and high impedance, to which buffer circuit the power source voltage is also applied, the output buffer circuit comprising a control circuit operable to switch the buffer circuit output state to the high impedance state in response to a control signal applied to the buffer circuit, characterised in that a detector circuit is provided in the output buffer circuit, in addition to the control circuit, which detector circuit is operable to detect an increase of the power source voltage applied to the buffer circuit and to switch the buffer circuit output state to the high impedance state in response to such detection."

Claims 2 to 8 are dependent upon Claim 1 and relate to:

- features (shown in figure 4) of a particular prior art output buffer circuit in which the claimed invention can be applied (Claim 2), and of its control circuit (Claim 8);
- features relating to the connection (Claim 3) and particularities of four embodiments of the detector circuit (Claims 4 to 7) shown in figures 6, 7a, 7b and 7c.

V. In the accompanying letter and during oral proceedings, held on the Appellant's request on 31 January 1989, he argued in particular with reference to D3 essentially as follows:

The claimed invention relates to a very narrow technological field, the switching of the output of a PROM output buffer to a high impedance state. In the prior art, this is done, in the writing mode, by applying a chip enable signal to a respective control input. The inventor has recognised other circumstances in which a high output impedance is required, namely when the power source voltage is, for whatever reasons, increased. In such a case, the output buffer transistors are, according to the invention, switched off to protect them against failure.

Nothing of this kind is suggested by D3 or any other prior art. Even if the problem had been recognised, it would only be obvious to solve it by other means, for instance prevention of voltage transients or use of more resilient transistors.

In D3b, there is no 1 to 1 relationship between the high Power Down/Program (PD/PGM) signal and the increased power source voltage (Vpp); cf. table I on page 309. "Power Down" refers to a standby mode during reading (figure 8) without relation to the source voltage. Even if "Program" refers to a writing operation in which the power source voltage is increased (page 313), the signal switching the output buffer into the high impedance state is not derived from the power source voltage. As a consequence of this latter fact, no switching off takes place if during reading operation the power source voltage is (for other reasons) increased.

Simple as the invention appears there is no perception in the prior art leading to it.

- VI. The Appellant requests to set aside the decision under appeal and grant a patent on the basis of the description, pages 1 to 6, 6a to 6c and 7 to 12 (with clerical errors amended), Claims 1 to 8 and drawings, sheet 1 to 3, all filed on 20 December 1988.

Reasons for the Decision

1. The appeal is admissible.
2. No formal objection arises against Claim 1, which is based on original Claim 9 as appended to Claim 2 and specified as disclosed in the description, or any of the other documents on file, disregarding clerical errors.
3. The subject-matter of Claim 1 is new but lacks an inventive step for the following reasons:

3.1 According to the preamble of Claim 1, the claimed invention sets out from a PROM device with an output buffer circuit having a control circuit as illustrated in figures 1 to 4. Its writing operation involves an increase in the power source voltage as described on page 7 last sentence. The output buffer is supplied with the same voltage, as described on page 8 first sentence. The control circuit (I, D1, D2), or chip enable circuit (18), switches the buffer output to a high impedance state during the writing operation, as is described on page 3 lines 5 to 14.

This arrangement is "conventional" (cf. description) or "prior art" (cf. drawing), although undocumented.

3.2 The prior art document on file coming nearest to this arrangement is D3, the other documents not relating to a possible application of their output buffers in a PROM device, i.e. with a read-only memory programmable by a writing operation.

D3, in particular D3b, also discloses all features of the preamble. The control circuit is described as an enable or select/deselect (CS) circuit turning, if false, or high, the output transistors off (page 311 first paragraph), i.e. in the high impedance state (table I) so that, in the programming mode, data to be written in cannot enter the output buffer from its output side but only the input buffer (cf. figure 5).

3.3 In addition, D3b discloses a second control circuit controlled by a different signal, "Power Down" in figure 6, but fully meaning "Power Down/Program" (PD/PGM). This PD/PGM control circuit is connected in parallel with the Chip Enable (CS) control circuit and thus has the same effect of switching the buffer output to a high impedance

state. It is activated however in two circumstances which the skilled person can clearly distinguish:

(a) Power Down:

In the reading operation for powering down the PROM (standby mode in figure 8).

(b) Program:

In the programming mode, or writing operation, when inter alia the power source voltage is increased, for allowing the data present on the output to be written into the selected address (page 309).

- 3.4 The Board agrees with the Appellant's submission that the "Power Down" aspect of the PD/PGM signal is not relevant to the claimed invention.

It further agrees that the subject-matter of Claim 1 differs from the known arrangement by the fact that, for the programming mode, the control signal for this second control circuit is directly derived from the power source voltage, an increase of the latter being the criterion for activating this circuit.

- 3.5 In the opinion of the Board, the skilled person must however be considered as being aware of the fact that, due to the direct nexus of an increased power source voltage with the programming mode (table I), a "Program" pulse to said second control circuit is directly derivable from the power source.

Even if it is agreed, that this applies only to the "Program" aspect and not to the "Power Down" aspect of the PD/PGM signal, the Board considers that it is obvious for the skilled person to disregard the Power Down mode if he

does not want to make use of it. Then he will use only the "Program" aspect in the aforementioned modified way.

- 3.6 In doing so, the skilled person would have arrived at the claimed invention, one of its uses being the case where in the programming mode (writing operation) the buffer output is required to take a high impedance state (page 7 last paragraph and page 8 until line 6).
- 3.7 It is agreed that the claimed invention has an additional, more general, effect, namely an extension of the high impedance output state from the writing mode alone to other modes, e.g. also the reading mode.

However, in accordance with the Examining Division's opinion, this more general effect is not a sufficient reason for drawing a different conclusion than the one arrived at under the foregoing item 3.6. It is only the evident logical consequence of the fact that the claimed invention constitutes, in effect, an extension of the "increase in power source voltage" for one reason, namely programming, to such an increase occurring for "other" reasons whatever these reasons may be. Clearly such other reasons for an excess voltage do exist and will be known to the skilled person although no example has been referred to in the description of the application. It will therefore be obvious to the skilled person that these cases may benefit from the same effect of turning the output transistors off as is required during programming with an increased voltage. This extended effect is not therefore surprising and cannot be taken as an indication for the presence of an inventive step.

This applies even more, if in practice it is found that an increased voltage, incidentally coinciding with another condition (page 6 last paragraph), would lead to

transistor failure, protecting circuits in general being common-place for such cases.

4. Claim 1 being unallowable for these reasons, there is no basis for allowing any of the dependent claims.

As to substance, these claims correspond to the Claims 3 to 9 the Examining Division rejected as lacking in inventive step, having regard to D2 (in particular figure 12) and to common practice. The Board sees no reason to question this finding. Consequently there is no ground to suggest a corresponding restriction of Claim 1.

Order

For these reasons, it is decided that:

The appeal is dismissed.

The Registrar:

The Chairman:

S. Fabiani

P.K.J. van den Berg