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Bezeichnung der Erfindung:
Title of invention:
Titre de l'invention : Improvements in or relating to sample-and-hold circuits and methods

Klassifikation / Classification / Classement : G11C 27/02

ENTSCHEIDUNG / DECISION

vom / of / du 12 December 1989

Anmelder / Applicant / Demandeur : Western Electric Company (US)

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Article 84

Schlagwort / Keyword / Mot clé : "Clarity of claim and support by the description"

Leitsatz / Headnote / Sommaire

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Case Number : T 128/88 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 12 December 1989

Appellant : Western Electric Company, Incorporated
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Representative : Buckley, Christopher Simon
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Decision under appeal : Decision of Examining Division 067 of the European Patent Office dated 2 November 1987 refusing European patent application No. 83 305 517.1 pursuant to Article 97(1) EPC

Composition of the Board :

Chairman : P.K.J. van den Berg
Members : W. Riewald
E. Persson

Summary of Facts and Submissions

I. European patent application No. 83 305 517.1, claiming priority of an application in the United States of 29 September 1982, filed on 20 September 1983 and published under No. 0 107 337, was refused by a decision of the Examining Division 067 dated 2 November 1987.

The decision was based on Claims 1 to 7 filed with letter of 17 September 1987.

II. The reason given for the refusal was that, although the application contained patentable subject-matter, the claims did not comply with the requirements of Article 84 EPC since Claim 1 was not clear and the presence of the two independent Claims 1 and 6 caused the claims not to be concise.

III. The prior art referred to in the application documents as filed is represented by

- a schematic circuit diagram depicted in Figure 1 of the application;

- D1: US-A-4 308 468;

- D2: IEEE-Journal of Solid-State Circuits, Vol. SC-16, No. 4, Aug. 1981, pages 367-371, "A Programmable Transversal Filter for Voice-Frequency Applications".

No further prior art documents were cited by the Examining Division.

IV. On 17 December 1987 the Appellant lodged an appeal against the decision of the Examining Division, the appeal fee having been paid on 14 December 1987. A Statement of Grounds of Appeal was received on 1 March 1988 together with a main request maintaining Claims 1 to 5 of 17 September 1987 (Claims 6 and 7 deleted) and an auxiliary request based on new Claims 1 to 5. The Appellant challenged the Examining Division's view in respect of the disputed clarity of Claim 1.

V. In the course of the proceedings before the Board, the Appellant amended the claims and the description, and finally requested that a patent be granted on the basis of the following application documents:

Description, pages 1 to 3 and 5 to 8 as published,
page 4, received with letter of
16 February 1989,
page 9, received with letter of
20 October 1989;

Claims 1 and 2, received with letter of 20 October 1989;

Drawings, sheet 1/2 as published,
sheet 2/2, received with letter of
16 February 1989.

VI. Claim 1 reads as follows:

"A sample-and-hold circuit including an amplifier (A) for receiving an input signal from an input signal node and a feedback signal from the output (16) of a buffer (B), a primary sampling switch (S_S) connected in a circuit path between the input signal node and an input (15) of the buffer (B), a primary holding capacitor (C_H) connected between the input of the buffer (B) and a reference

potential point, and CHARACTERISED BY correction sample-and-hold means including a correction holding capacitor (C_{CH}) having one side connected through a correction sampling switch (S_C) to the output (14) of the amplifier (A), and the other side connected to a reference potential point, a correction coupling capacitor (C_{CC}) for coupling a correction signal from the one side of the correction holding capacitor (C_{CH}) to the primary holding capacitor, the correction coupling capacitor (C_{CC}) having a capacitance substantially less than that of the primary holding capacitor (C_H), and control means for keeping the correction sampling switch (S_C) closed for a predetermined period of time after opening of the primary sampling switch (S_S) in order to provide a correction of a change in the level of the signal on the primary holding capacitor (C_H) caused by the switching feedthrough error resulting from the opening of the primary sampling switch."

Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is admissible.

2. Novelty.

In its precharacterising portion, Claim 1 starts from a prior art as disclosed in Figure 1 of the application with sample-and-hold means comprising a primary sampling switch (S_S) and a primary holding capacitor (C_H) together with an input amplifier (A) and an output buffer (B).

The sample-and-hold circuit of Claim 1 differs therefrom by the addition of correction sample-and-hold means including (see Figure 2) a correction sampling switch (S_C), a

correction holding capacitor (C_{CH}) and a correction coupling capacitor (C_{CC}) together with appropriate control means.

Documents D1 and D2, cited and acknowledged in the present description, page 3, line 13 to page 4, line 1, do not disclose such correction sample-and-hold means.

3. Clarity of Claim 1 and its support by the description.

3.1 The problem to be solved by the present invention arises from the fact that in known sample-and-hold circuits, as described in connection with Figure 1 of the application, a so-called "switching charge feedthrough" causes a "hold voltage offset" that falsifies the signal output. The voltage of the holding capacitor, that equals the voltage to be sampled just before the sampling switch opens, undergoes a change when the sampling switch opens. This change is caused by a capacitive coupling between the control input of the sampling switch and its terminals (e.g. gate, source and drain of an MOS device); cf. description, page 2, line 32 to page 3, line 12.

With the features now specified in Claim 1 all the objections as to clarity of the claim are overcome as set out in the following.

3.2 The connection of both the input signal from an input signal source and of the feedback signal from the output of the buffer as input signals to the amplifier (point 2 of the Examining Division's communication of 26 June 1987) is now clarified in lines 2 to 4 of Claim 1.

3.3 The connection of the primary sampling switch is, in accordance with the original Claim 1, specified as being

made in a circuit path between the input signal node and the input of the buffer.

The Board is satisfied that it is not necessary to specify in Claim 1 that the input of the primary sampling switch is connected to the output of the amplifier (in contrast to the suggestion in point 2 of the Examining Division's communication of 26 June 1987 and the Rapporteur's suggested claim in the communication of 27 October 1988). The Board agrees to the Appellant's broader wording of Claim 1 in this respect, as requested with letter of 16 February 1989, point 2 for the following reasons:

The present invention realises a concept in which, in a first step, the primary holding capacitor of a sample-and-hold circuit is to be charged to a voltage approximately equal to the input voltage.

Remaining small differences to the input voltage can be lowered, in a second step, by the correction sample-and-hold circuit which has to compensate or counteract the error voltage on holding capacitor C_H. The amplifier and feedback arrangement as well as the attenuation means are necessary means for this function. However, it is clear that the first step, i.e. the charging of the primary holding capacitor to only approximately the input voltage, can already be effected by a sample-and-hold circuit in its simpler form, i.e. without an amplifier and feedback arrangement as known, for instance, from D1 (US-A-4 308 468) cited in the present application. It is therefore agreed that a corresponding embodiment with a connection of the primary sampling switch directly to the input signal node should not be excluded from the scope of Claim 1.

3.4 The necessary details of the correction sample-and-hold means, viz. the circuitry comprising the correction sampling switch (S_C), the correction holding capacitor (C_{CH}) and the correction coupling capacitor (C_{CC}), originally specified in Claims 2 and 3, are now incorporated in Claim 1, as suggested in the Examining Division's communication of 26 June 1987, points 4 and 5 and in the communications of the Board.

3.5 Claim 1 now also specifies the necessary timing of the two sampling switches (see the Examining Division's communication of 26 June 1987, point 4) in accordance with the description of the operation mode on page 6, line 33 to page 7, line 8: The correction sample-and-hold means are activated by keeping the correction sampling switch (S_C) closed for a predetermined period of time after opening of the primary sampling switch (S_S), thereby maintaining a feedback loop that provides the correction of the feedthrough error resulting from the opening of the primary sampling switch.

3.6 Consequently, Claim 1, in its present form, is sufficiently clear. All the features incorporated in the claim are disclosed in the description. Therefore, Claim 1 is also supported by the description.

3.7 All the amendments made are clearly based on the original disclosure so that there is no objection under Article 123(2) EPC.

4. Inventive step.

A solution to the problem how to compensate for the "hold voltage offset" caused by the "switching charge feedthrough" of the sampling switch is known from document D1 (US-A-4 308 468) and acknowledged as prior art in the

application on page 3, line 13 onwards. According to this document a charge feedthrough compensation switch 10 is connected across the sampling switch 2. The function of this compensation switch 10 is completely different from the function of the presently claimed "correction sampling switch", because the compensation switch is negatively biased so that it is always open (D1, column 2, lines 14 to 22). The only purpose of the switch 10 is to create a second charge feedthrough current of opposite polarity that cancels the charge feedthrough current caused by the control pulse on the virtual sampling switch 2 (D1, column 2, lines 23 to 26). This solution to the problem would, without any change, also be applicable in a sample-and-hold circuit with a feedback loop according to Figure 1 of the application.

However, the Applicant did not follow this known concept or any similar line. Instead, he has found a surprising new concept by a further development of the feedback concept. He has conceived a correction sample-and-hold means including a correction holding capacitor and a correction sampling switch that, at first sight, does not differ from the primary sample-and-hold means. The inventive idea is that, after the primary sample-and-hold means have caused a preliminary charge of the primary holding capacitor, a remaining error in this charge (caused by the switching feedthrough current) can be corrected by maintaining for a predetermined period of time the feedback circuit in a modified way. The modification is to be seen in the capacitive coupling of the correction sample-and-hold means to the primary holding capacitor via the correction coupling capacitor which provides an attenuation of the effect of the offset voltage caused by the opening of the correction sampling switch (see description, page 6, line 33 to page 4, line 16).

This novel concept is not derivable from document D2 either which discusses the problem of fixed pattern noise in a configuration of a bank of feedback sample-and-hold circuits caused by variations in the net charge feedthrough of the sampling switches and any compensating switches. The compensating technique is, in this case, based on providing a "differential sample-and-hold circuit" (Figure 2): two sample-and-hold circuits are arranged physically very close to each other, one for storing a bias voltage and the other for storing the signal plus bias (page 368, right-hand column, second paragraph).

The Examining Division has not discussed any further documents cited in the search report. The Board has checked these documents and agrees with the implicit view of the first instance that these documents do not provide prior art that comes nearer to the claimed subject-matter than the prior art acknowledged in the introductory part of the present description.

The subject-matter of Claim 1 is therefore considered as involving an inventive step.

5. Claim 2 is a dependent claim specifying a particular embodiment of the subject-matter of Claim 1 and thus also meets the requirements of novelty and inventive step.

The original independent Claim 6 being deleted, there is no longer an objection as to lack of conciseness of the claims.

6. Consequently, the application documents presently on file are no longer open to the objections made by the first instance.

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a European patent with the documents specified in section V.

The Registrar: The Chairman:

S. Fabiani P.K.J. van den Berg