

Veröffentlichung im Amtsblatt	Ja/Nein
Publication in the Official Journal	Yes/No
Publication au Journal Officiel	Oui/Non



Aktenzeichen / Case Number / N° du recours : T 165/88 - 3.5.1

Anmeldenummer / Filing No / N° de la demande : 82 109 186.5

Veröffentlichungs-Nr. / Publication No / N° de la publication : 0 078 916

Bezeichnung der Erfindung: Shared TOD clock modification bit

Title of invention:

Titre de l'invention :

Klassifikation / Classification / Classement : G06F 3/00, G06F 9/46

### ENTSCHEIDUNG / DECISION

vom / of / du 14 December 1988

Anmelder / Applicant / Demandeur : IBM Corp.

Patentinhaber / Proprietor of the patent /  
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPU / EPC / CBE Article 83

Schlagwort / Keyword / Mot clé : Insufficient disclosure

Leitsatz / Headnote / Sommaire

Europäisches  
Patentamt

Beschwerdekammern

European Patent  
Office

Boards of Appeal

Office européen  
des brevets

Chambres de recours



Case Number : T 165/88

**D E C I S I O N**  
of the Technical Board of Appeal  
of 14 December 1988

**Appellant :** International Business Machines Corporation  
Armonk, N.Y. 10504 (US)

**Representative :** Jost; Ottokarl, Dipl.Ing.  
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**Decision under appeal :** Decision of Examining Division 065  
of the European Patent Office  
dated 10 November 1987 refusing  
European patent application  
No. 82 109 186.5 pursuant to  
Article 97(1) EPC

**Composition of the Board :**

**Chairman :** P.K.J. van den Berg

**Members :** W.P.H. Riewald

F. Benussi

## Summary of Facts and Submissions

- I. European patent application No. 82 109 186.5 was filed on 5 October 1982, claiming priority from a US application of 10 November 1981.

The application was refused by a decision of the Examining Division dated 10 November 1987.

The reason given for the refusal was that the application did not sufficiently disclose the invention as required by Article 83 EPC.

- II. The Appellant filed a notice of appeal on 23 December 1987, paid the appeal fee on 12 January 1988 and filed a statement of grounds of appeal on 10 March 1988 accompanied by new Claims 1 and 2 and amended parts of the description and drawings.

The Appellant requests to cancel the decision and grant a European patent on the basis of the amended documents.

- III. The decision is based on the following documents:

description, pages 1, 4 to 7 and 8, filed with letter of 4 March 1988;

description, pages 2 and 9 as published;

description, pages 3 and 7a, filed with letter of 8 May 1987;

Claims 1 and 2, filed with letter of 4 March 1988;

drawings, sheets 1, 7 and 8, filed with letter of 4 March 1988;

drawings, sheets 2 to 6 as published.

The independent claims read as follows:

"1. In a computer which has a TOD clock count maintained in a TOD clock register (14) that is shared by at least two processors (10, 12) where each processor implements a timer function by subtracting a stored count from a count of the TOD clock register and where at least one processor is capable of changing the TOD count in the TOD clock register by instructions (STP), (STPT) and at the completion thereof updating the stored counts for the processor using a respective TOD value, a method for correcting errors introduced into the timer calculations of the other processor by a concurrently occurring change in the TOD clock count made by said one processor, characterized by

storing one type of binary manifestation (Bit 61 = ON) as a status signal in said TOD clock register along with the TOD count each time the TOD clock is changed by said one processor which is changing the TOD count;

supplying said one type of binary manifestation (Bit 61 = ON) to said other processor only the first time it interrogates said TOD clock register after said TOD clock register has been modified by said first processor or vice versa;

modifying the first occurring timer calculation of said other processor by said stored respective TOD value which reflects the magnitude of any error which

exists in the timer calculation as a result of said changing of the TOD clock count in said TOD clock register.

2. A method of correcting all errors introduced into timer calculations of two processors which implement timer calculations by subtracting a stored count maintained separately by each processor from a TOD clock count maintained in the shared TOD clock register (14) when one processor changes the TOD count in said TOD register comprising:

storing the difference (TOD ) between the TOD clock counts before and after it has been changed by the one processor, storing one type of binary manifestation (Bit 61 = ON) as a status signal in said TOD clock register along with the TOD count when the TOD count is changed by said one processor,

updating the stored counts in both processors to reflect the change in the TOD clock prior to the start of the next operation of each processor by subtracting the difference (TOD ) stored previously from the stored counts,

changing the difference (TOD ) stored to zero after the stored counts in both processors have been updated to reflect the updated condition of the stored counts,

modifying the first timer calculation of the other processor to occur after the storing of the one manifestation (Bit 61 = ON) by subtracting the difference (TOD ) stored from the calculation to prevent errors in timer calculations in said other

processor which occurred concurrently with the change in the TOD count, and

changing the status signal to another binary manifestation (Bit 61 = OFF) to reflect the fact that the TOD clock has not been changed in the TOD clock register since the last timer calculation of the other processor.

IV. The arguments of the Examining Division in the examining procedure can be summarised as follows:

According to the disclosure of the present application, two kinds of bits are generated together with the modification of the common TOD clock by an SCK (set clock) instruction from one of two processors: Bits 24 and 26 are stored in each processor. A bit 61 is stored in the system controller 15 common to both processors.

It seems that the bits 24 and 26 are used to update respective timer parameters in the processors in accordance with the modified TOD clock at the end (EOP) of any next current instruction of the processors.

This mechanism seems to work except when an SPT ("Set CPU Timer") or STPT ("Store CPU Timer") instruction is that next current instruction in either processor. Therefore, Bit 61 seems to be additionally provided.

Bit 61 seems to be set only when one processor first reads the TOD register after a change of the TOD by an SCK instruction from the other processor. Thus, only the processor that has not changed the TOD is able to use the Bit 61 during execution of SPT or STPT to correct the timing function of its CPU timer. Therefore, in the application as filed there is given no solution for the

case where an SPT or STPT instruction follows immediately an SCK instruction in the same processor.

- V. The Appellant's counter arguments can be summarised as follows:

The Examiner's understanding of the function of bits 24 and 26 is not correct. These bits signal all CPU's the TOD clock change and the adjustment of the CPU timers is done by this internal signalling system directly, i.e. prior to an EOP instruction.

This direct adjustment of the CPU timers in accordance with a change in the TOD clock via a CPU-to-CPU signalling mechanism is accomplished by an SIG P function which is prior art.

In contrast to this, the purpose of the invention is directed at eliminating the problem caused by errors introduced into the timer calculations if an SPT or an STPT instruction is being executed on one processor while the other processor is performing a set TOD clock instruction.

- VI. The Examining Division maintained in its decision the view that neither the claims nor the description make fully clear how the bits 24, 26 or 61, respectively, are used and that there is given no solution for the case where an SPT or an STPT instruction follows immediately an SCK instruction in the same processor.

The newly introduced function SIG P as adjusting the CPU timers is regarded as contrary to the description as filed, which clearly indicates that the processor executing the SCK instruction only signals to all CPUs that the TOD has changed and that each CPU updates the timers only at the end of a current unit of operation (EOP).

VII. The Appellant's arguments stated in the grounds of appeal can be summarised as follows:

The obscurities in the application documents seem to be clarified by the amendments introduced into the newly filed documents.

Since the main part of the description deals with the problem of malfunctioning if either one of the instructions SPT or STPT is being executed on one CPU while the other CPU is performing an SCK instruction, it is not necessary to refer precisely to the modification bits 24, 26 and 61. The presented more general explanation should suffice.

The function SIG P, as presented in Figure 2A, is to be regarded as standard processor routine in the prior art.

#### Reasons for the Decision

1. The appeal is admissible.
2. The application does not disclose the invention in a manner sufficiently clear and complete for it to be carried out by a person skilled in the art, as required by Article 83 EPC.
  - 2.1 The application relates to a multiprocessing system with a single time-of-day (TOD) clock which is shared by at least two central processing units (CPUs). Each CPU is provided with a CPU timer which can be implemented as a function of the TOD clock. To do this, each CPU maintains a parameter in local store which is, when the timer is set (SPT instruction), calculated by adding a preselected amount to the reading on the TOD clock. The timer value can then be

computed by subtracting a later reading of the TOD clock from the local store parameter (page 1, first and second paragraphs).

Each CPU has the capability to set the shared TOD clock (SCK instruction). When such an instruction, which modifies the TOD clock, is executed, the stored CPU timer parameters in both CPUs must be adjusted. The last paragraph of page 1 of the description states in this context:

"The issuing CPU ... signals all CPUs of the TOD clock change via a CPU-to-CPU signalling mechanism. At the end of the current unit operation (EOP), each CPU will execute a ... TOD Clock Change Handler routine ... to update its CPU timer parameter ...".

From page 5 (as originally filed), lines 21 to 28 can be understood that only the signalling of the TOD clock change is executed by the bits 24, 26, whereas the last paragraph of page 5 confirms the fact that the adjustment is only made at the end of "the next current unit operation (EOP)".

The Board is therefore satisfied that the Examining Division is right in respect of the disclosed function of the bits 24 and 26, and that the Appellant's argument that the adjustment is done prior to the EOP is not consistent with the original disclosure. The Appellant's reference to the SIG P function is not suitable to substantiate his contention. This SIG P function is indicated only in a block of the TOD Clock Change Handler routine in Figure 2 and not explained in the description. The allegation that this function SIG P is to be regarded as a standard processor routine is not supported by a clear citation from the prior art. Nor can it be seen that a closer

specification could change the fact that, according to page 5, last paragraph, the whole microcode shown in Figure 2 is not involved before the end of the "next current unit operation (EOP)".

- 2.2 The function of the Bit 61 must now be seen in connection with the problem of avoiding errors introduced into the CPU timer calculation if an SPT ("Set CPU Timer") instructions or an STPT ("Store CPU Timer) instruction is to be executed on one processor while the other processor is modifying the TOD clock value by an SCK ("Set Clock") instruction.

It can be understood from page 6, second paragraph of the description that the difficulty arises that the one processor may carry out a calculation based on a stored timer parameter in accordance with the TOD setting prior to the SCK instruction and on a current TOD clock value derived from the TOD register after the SCK instruction, i.e. based on a modified TOD setting. The Bit 61 as part of the TOD register contents is intended to indicate this "error" situation in order to allow a correction of the error by a TOD signal which reflects the change of the TOD value in response to the SCK instruction.

It is clear that Bit 61 must exactly reflect the said "error" condition. This requires the identification of the timing of

- (a) the change of the setting of the TOD clock register,
- (b) the change of the timer parameter stored in the respective CPU in response to the change of the setting of the TOD clock register.

Only between these two points of time the said correction must be carried out. It follows from what is stated in

section 2.1 above that, in particular, the timing of the parameter change is not clear from the present description. This timing depends not only on the somewhat vague meaning of "end of the current unit of operation (EOP)" but also on the timing details of the "TOD Clock Change Handler routine" which updates the CPU timer parameter (Figure 2 of the application).

Therefore, already the preconditions necessary to clarify the problem are not clearly disclosed in the application. Likewise, the details of Figure 4 showing the logic of Bit 61-generation are not suitable to clarify the situation since they also do not reflect the timing of the timer parameter change in the respective CPUs.

The Appellant's line of argument, that any obscurities can be remedied by reference to the fact that the correct details are prior art cannot be accepted. As far as the correct description of the prior art is necessary for understanding the invention, this must be done in the application as filed in an unambiguous way that does not admit of any doubt.

- 2.3 Therefore, the Appellant's submission that it would not be necessary to have a precise description of the operation by referring precisely to the modification bits 24, 26 and 61 since the inventive mechanism is sufficiently dealt with, is not well founded.

The Board has taken into account the amendments introduced by the Appellant into the application documents filed with the submission of the grounds of appeal and comes to the conclusion that they only concern minor clarifications and do not affect the main objections brought forward by the Examining Division.

The application does not satisfy the requirements of Article 83 EPC.

The refusal of the application by the Examining Division on the ground of insufficient disclosure of the invention was justified.

Order

For these reasons, it is decided that:

The appeal is dismissed.

The Registrar:

The Chairman:

S. Fabiani

P.K.J. van den Berg