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Veröffentlichung im Amtsblatt	Ja/Nein
Publication in the Official Journal	Yes/No
Publication au Journal Officiel	Oui/Non

Aktenzeichen / Case Number / N° du recours : T 351/88 - 3.5.1

Anmeldenummer / Filing No / N° de la demande : 80 105 584.9

Veröffentlichungs-Nr. / Publication No / N° de la publication :

Bezeichnung der Erfindung: Semiconductor memory device
Title of invention:
Titre de l'invention :

Klassifikation / Classification / Classement : G11C 11/40

ENTSCHEIDUNG / DECISION
vom / of / du 3 July 1990

Anmelder / Applicant / Demandeur : Tokyo Shibaura Denki Kabushiki Kaisha

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Article 56

Schlagwort / Keyword / Mot clé : "Inventive step (no)"

Leitsatz / Headnote / Sommaire

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Case Number : T 351/88 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 3 July 1990

Appellant : Tokyo Shibaura Denki Kabishiki Kaisha
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Decision under appeal : Decision of Examining Division 067 of the European Patent Office dated 25 November 1987 refusing European patent application No. 80 105 584.9 pursuant to Article 97(1) EPC

Composition of the Board :

Chairman : E. Persson
Members : Y. van Henden
W. Wheeler

Summary of Facts and Submissions

I. European patent application No. 80 105 584.9, filed on 17 September 1980 and claiming priority from four previous applications in Japan dated 19 September 1979, 4 October 1979 and 17 April 1980, was refused by a decision of the Examining Division dated 25 November 1987. That decision was taken on the basis of Claims 1 to 3 received on 25 June 1987.

II. The reason given for the refusal was that, having regard to the state of the art disclosed in documents

D1: JP-A-53/148 398 &
D2: US-A-4 209 716,

the subject-matter of the claims did not involve an inventive step.

III. The Appellant filed on 18 December 1987 a notice of appeal against the decision of the Examining Division and simultaneously paid the corresponding fee. An amended version of said notice was filed on 7 January 1988 and the statement of grounds was received on 25 March 1988, together with new Claims 1 to 3 to replace the previous ones.

IV. In a communication pursuant to Article 11(2) of the Rules of Procedure of the Boards of Appeal, the Rapporteur of the Board explained that, having regard to the state of the art disclosed in (D1), as interpreted with the aid of document (D2), which the Appellant accepts to be identical in content with (D1), the subject-matter of the claims submitted with the Statement of Grounds of Appeal could not be credited with an inventive step.

V. With letter of 8 June 1990, the Appellant submitted a single claim to replace those previously on file. Said claim is worded as follows:

"A semiconductor device comprising:

a first semiconductor region (42) and first to fourth memory cell forming areas (I-IV) all formed in a semiconductor substrate (41) of a first conductivity type,

said first semiconductor region (42) having a second conductivity type opposite to said first conductivity type and including a center region (C) and first to fourth extension regions (42d, 42a, 42b, 42c) which extend in four directions away from said center region (C), with the first and third extensions formed along a row direction and the second and fourth extensions formed along a column direction, thereby dividing the major surface of said semiconductor substrate (41) into said first and second, second and third, third and fourth, fourth and first extensions, respectively, said first cell forming area including:

a second semiconductor region (45) of said second conductivity type having one end formed proximate extremity of said first extension region (42d) which is provided in said row direction, for forming a first driver transistor (Q1) having a first channel region between said second semiconductor region (45) and said first extension region (42d);

a third semiconductor region (43) of said second conductivity type formed proximate extremity of said second extension region (42a) which is provided in said column direction, for forming a second driver transistor (Q2) having a second channel region between said third semiconductor region (48) and said second extension region (42);

a fourth semiconductor region (47) of said second conductivity type formed close to the other end of said second semiconductor region (45) for forming a first switching transistor (Q3) having a third channel region between said fourth semiconductor region (47) and said second semiconductor region (45) and extending in parallel to said second extension region (42a);

fifth and sixth semiconductor regions (48,49) of said second conductivity type formed close to each other, for forming a second switching transistor (Q4) having a fourth channel region therebetween and aligned in parallel to the first switching transistor (Q3),

a first polycrystalline silicon gate electrode (46) including a first portion formed above said first channel region between said first extension region (42d) and said one end of said second semiconductor region (45) and being the gate electrode of said first driver transistor (Q1), one end of said first gate electrode (46) extending in said column direction and being in connection to said fifth semiconductor region (48), and the other end of said first gate electrode (46) extending to be connected to said third semiconductor region (43);

a second polycrystalline silicon gate electrode (44) including a second portion formed above said second channel region between said second extension region (42a) and said third semiconductor region (43) and being the gate electrode of said second driver transistor (Q2), one end of said second gate electrode (44) extending to be connected to said second semiconductor region (45);

a polycrystalline silicon word line (Wl) formed in the row direction on a gate insulation layer and being a common gate electrode of said first and second switching transistors (Q3,Q4);

a first resistance polycrystalline silicon layer (R2), including a first high resistance portion formed above said first portion of said first polycrystalline

silicon gate electrode (46) on an insulation layer therebetween, said first resistance layer (R2) having a first connection portion, one end of which is in contact with a junction of said fifth semiconductor region (48) and said first polycrystalline silicon gate electrode (46) such that said first high resistance portion is used as a load for said second driver transistor (Q2);

a second resistance polycrystalline silicon layer (R1), including a second high resistance portion formed above said second portion of said second polycrystalline gate electrode (44) on an insulation layer therebetween, said second resistance layer (R1) having a second connecting portion, one end of which is in contact with a junction of said second semiconductor region (45) and said second polycrystalline silicon gate electrode (44) such that said second high resistance portion is used as a load for said first driver transistor (Q1);

a metal ground line (Vss) formed in the column direction on an insulation layer so as to pass above said center region (C) for connection with said first semiconductor region (42); and

first and second metal data lines (D1,D1) formed in the column direction and connected, respectively, to said first and second switching transistors (Q3,Q4),

characterized in that

said first and second memory cell forming areas are substantially mirror images of each other about said second extension, said second and third memory cell forming areas are substantially mirror images of each other about said third extension, said third and fourth memory cell forming areas are substantially mirror images of each other about said fourth extension, and said fourth and first memory cell forming areas are substantially mirror images of each other about said first extension."

VI. Oral proceedings were held on 3 July 1990.

VII. The Appellant requests that the decision under appeal be set aside and a patent granted on the basis of the claim filed with his letter of 8 June 1990.

VIII. To support his view, the Appellant submitted that, owing to the symmetrical arrangement of the memory cells, stray capacitances which are formed between load resistances and gate electrodes of the driver transistors will have substantially the same value. Therefore, no imbalance of data holding will occur at any memory element formed on the semiconductor wafer. Additionally, the symmetrical arrangement provides constant data discharge and restoration times.

Reasons for the Decision

1. The appeal is admissible.

2. Despite certain grammatical deficiencies exhibited by the wording of the claim submitted by the Appellant, the Board holds it for clear. It is indeed not necessary to refer to the description and drawings to interpret the claim.

3. **Novelty**

3.1 Document (D1) claims inter alia the priority of the US patent application No. 746 665, filed on 2 December 1976 and on which (D2) was granted. The drawings of (D1) being identical to those of (D2), it was submitted that the part of (D1) referring to the drawings is a translation of the section of (D2) headed "detailed description of specific embodiment". The Appellant did not contest the validity of this inference and it may be accepted that, although (D2) was issued later than the priority date of the present

application, the content of said detailed description had been made available to the public before said priority date by the publication of (D1) on 23 December 1978 and thus belongs to prior art - Article 54(2) EPC.

3.2 Taking into consideration the Figures 1 to 3d and the detailed description of (D2), the claimed subject-matter appears to distinguish over the prior art known from (D1) in that:

- the first semiconductor region (42) includes a centre region (C) and first to fourth extension regions which extend away from said centre region, two along a row direction and two along a column direction, thereby dividing the major surface of the substrate into first to fourth memory cell areas (I-IV);

- the memory cells formed on respective sides of each extension region are substantially mirror images of each other with respect to said extension region;

- the ground line Vss is a metal strip formed in the column direction on an insulation layer so as to pass above the centre region (C) for connection with the first semiconductor region (42), and

- in that the portion of the first gate electrode (46) underlying the resistive portion of the layer (R2) is located above the channel region of the first driver transistor (Q1).

Furthermore, the features referenced (30, 10, 11+12, 14, 13, 32, 17, 21, 29, 12, 23+24, R1, R2, Q1, Q2, Q3, Q4) in the illustration of prior art respectively correspond to those referenced (41, 42a, 42d, 45, 43, 47, 46, 44, W1, Vss, D1+D1, R1, R2, Q1, Q2, Q3, Q4) in the claim - see

(D2): from column 2, line 47 to column 3, line 50; from column 6, line 57 to column 7, line 2; column 8, lines 31 to 50; note also that although no references are attributed in (D2) to the fifth and sixth semiconductor regions, they are present as part of the structure of transistors (Q3) and (Q4).

4. **Inventive step**

4.1 No inventive step can be perceived in setting the problem for which a solution is proposed in the application.

Seeking to increase the packaging density of semiconductor memory devices is indeed a main concern of skilled people working in the field of integrated circuits, since both memory capacity and operation speed are thereby increased, whereas power consumption is lowered - see, in D2, the lines 56 to 59 of column 3 and the lines 6 to 9 of column 5. Furthermore, it is an object of anyone working in the field of electronics to obviate or at least alleviate the effects of stray capacitances.

4.2 Document (D2) teaches that a considerable economy of space would be achieved by mirroring the cell of Figure 1 about an axis (55) to define the cell on the right of the one shown, and by mirroring the cell about an axis (57) to define the cell below it, whereby adjacent cells would share the Vcc and Vss lines - see column 8, lines 31 to 39. As can be seen in Figure 1, the axis (55) is parallel to the column direction and substantially equidistant to the edges of a first region (10), whereas the axis (57) is not represented. Nevertheless, the skilled man reading (D2) readily understands that the cell represented in Figure 1 and the one located below would not share the Vcc and Vss lines if the axis (57) were not parallel to the row direction and located within both of said lines.

Likewise, he need not display inventive talent to understand that no place would be spared if the axis (57) were not substantially equidistant to the edges of the Vcc and Vss lines.

Bearing in mind that the substrate of the device disclosed in (D1) is of the p type silicon and that the regions (10, 11, 12) are of n^+ conductivity type, i.e. the first and second conductivity types referred to in the application, it thus appears that, without being involved in the exercise of inventive ingenuity, the skilled man carrying out the teaching of (D1) is led to make a semiconductor memory device with a substrate comprising a region having a conductivity type opposite to that of the substrate, which region includes a centre region, a first (11, 12, mirror image of 11 with respect to the axis 57) and a third extension region formed along a row direction and extending away from said centre region, and a second (10) and a fourth extension region formed along a column direction and extending away from the centre region, said extension regions dividing the substrate surface into four areas on which are formed memory cells and the memory cells adjacent any one of the extension regions being mirror images of each other with respect to said extension region. With regard to the Appellant's submissions of 8 June 1990, it may not be denied that such a device would achieve the results expected from the invention.

4.3 Providing a Vss line in the form of a metal strip on an insulating layer instead of, for instance, a polycrystalline silicon strip being an integral part of the first semiconductor region, as known from (D1), is considered by the Board to lie within the competence of the average skilled person and not liable to give rise to any unexpected advantageous effect that might be considered as evidence of an inventive step. As a matter

of fact, no such effect is mentioned in the application and the Appellant did not dispute that point.

4.4 The application as filed does not reveal the slightest information leading the reader to think that providing the resistive portions (R1,R2) above those parts of the gate electrodes (44,46) that overly the channel regions of the driver transistors (Q2,Q1), respectively, would ensure the achievement of better results than providing said resistive regions above other parts of said electrodes. Furthermore, it is noteworthy that the memory device according to Figure 2 of the application as filed, where no resistive portions are provided, is also deemed to achieve the purpose of the invention. An additional reason not to credit the above feature, i.e. the location of the resistive portions above the gate electrodes, with an inventive step is that capacitances also depend on a plurality of parameters whose values cannot be inferred from the application, in particular the areas of facing conductor portions, the thickness of the dielectric layers separating said portions and their dielectric constant.

4.5 The arguments put forward in Appellant's letter dated 8 June 1990 and during the oral proceedings do not invalidate above conclusions. Mirroring is indeed the first solution the skilled man will envisage if testing memory devices reveals imbalance effects between adjacent cells. Furthermore, this principle and one of the advantages it offers are known from (D1).

4.6 The subject-matter of the claim received on 8 June 1990 lacks an inventive step - Article 56 EPC.

5. The claim on file is not allowable - Article 52(1) EPC.

Order

For these reasons, it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

M. Kiehl E. Persson