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Bezeichnung der Erfindung:
Title of invention:
Titre de l'invention : Recirculating loop memory array with a shift register buffer

Klassifikation / Classification / Classement : G11C 19/28

ENTSCHEIDUNG / DECISION

vom / of / du 13 August 1990

Anmelder / Applicant / Demandeur : International Business Machines Corporation

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Art. 54, 56

Schlagwort / Keyword / Mot clé : "Inventive step (yes)"

Leitsatz / Headnote / Sommaire

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Case Number : T 425/88 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 13 August 1990

Appellant : International Business Machines Corporation
Old Orchard Road
Armonk, N.Y. 10504
US

Representative : Böhmer, Hans Erich, Dipl.-Ing
Keplerstraße 23
D - 7042 Aidlingen-Dachtel

Decision under appeal : Decision of Examining Division 067 of the European Patent Office dated 25 May 1988 refusing European patent application No. 81 106 231.4 pursuant to Article 97(1) EPC

Composition of the Board :

Chairman : P. van den Berg
Members : A. Clelland
M. Lewenton

Summary of Facts and Submissions

I. Appellant's European patent application No. 81 106 231.4, filed on 10 August 1981, claiming priority from a previous application in the United States of America dated 30 September 1980, was refused by a decision of the Examining Division dated 25 May 1988. The decision was based on Claims 1 to 5 as filed with a letter dated 14 August 1987.

II. The reason given for the refusal was that the subject-matter of Claim 1 lacked an inventive step having regard to the prior art known from the following documents:

D1: IBM Technical Disclosure Bulletin, Vol. 13, No. 7, December 1970, page 1879, and

D2: L'Onde Electrique, Vol. 58, No. 4, April 1978, pages 312-318.

III. On 19 July 1988 the Appellant filed a Notice of Appeal and Statement of Grounds against the decision, together with the appeal fee.

IV. In response to a communication of the Board pursuant to Article 110(2) EPC, the Appellant, in a letter dated 29 March 1990, maintained the existing Claim 1 with minor amendment and filed a further Claim 1 as an auxiliary request.

V. Oral proceedings were held on 10 May 1990.

In these proceedings the Appellant withdrew the existing auxiliary request and presented a new auxiliary request.

In the course of the oral proceedings, the Board held that Claim 1 of both the main and auxiliary requests failed to comply with Article 84 EPC as to clarity. It appeared however that the application included inventive subject-matter and the Board, therefore, took the decision to continue the procedure in writing in order to give the Appellant the opportunity to present a clarified Claim 1.

VI. With a letter dated 28 June 1990 the Appellant presented a revised Claim 1 and revised introduction to the description.

The Appellant now requests that the decision under appeal be set aside and that a patent be granted on the basis of the following documents:

Description:
pages 4-7 as originally filed
pages 1-3 as filed with the letter of 28.06.90

Claims:
Claim 1 as filed with the letter of 28.06.90
Claims 2-5 as filed with the letter of 14.08.87

Drawings:
sheets 1/2, 2/2 as originally filed.

VII. Claim 1 as now presented reads as follows:

"A memory array including a plurality of recirculating memory elements (1, 2 ...N), said memory elements being clocked in synchronism, so that the corresponding bits recirculate in their respective loops with the same time phase, and a shift register (7) having a number of cells (1', 2' ... N') equal in number to the number of said memory elements, characterized by first input means (17,

27, 29) for selectively connecting each cell to a respective one of said memory elements for simultaneously writing data into said memory elements in parallel, first output means (16, 30, 31) for selectively connecting each cell to a respective one of said memory elements for simultaneously reading data from said memory elements in parallel, and by control means (13, 15) for clocking and shifting data into or out of said shift register through all the cells in the time interval between successive clocking steps of said memory elements."

VIII. The Appellant's submission in support of an inventive step can be summarised as follows:

D1 discloses a particular form of recirculating shift registers and with a fixed 1:2 ratio of clock frequencies between the cells of the recirculating registers and the input register. The skilled man would have no good reason to alter this ratio to arrive at that required by Claim 1. The physical construction is, moreover, quite different to that of the invention and any similarity is only apparent with the benefit of hindsight. The skilled man would have no reason to read the disclosure of D2 in combination with that of D1 and even if he did so would not arrive at the claimed memory array.

Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is, therefore, admissible.

2. An examination of patentability of the subject-matter of amended claims presupposes that the amendments are admissible, in particular that they do not contravene Article 123(2) EPC. Claim 1 includes a feature not

explicitly present in the originally filed application, namely that the shift register cells are written to, and read from, respective memory elements simultaneously, the application as filed merely referring to reading and writing to the memory elements in parallel. That the reference to "in parallel" means in the context "simultaneously" can be directly and unambiguously derived from Figure 1, in which the so-called parallel read and write lines 16 and 17 respectively are each connected to each shift register cell, so that reading and writing to all the cells will occur simultaneously. Claim 1 is, therefore, admissible.

3. The application is concerned with providing fast and efficient data transfer into and out of a memory array including a plurality of recirculating memory elements, in particular CCD loops of the so-called "SPS" type in which data is continually recirculated in an arrangement consisting of a first, "serial" shift register, each cell of this shift register being connected to a first cell of a respective "parallel" shift register, the last cell of which is in turn connected to a respective cell of a further "serial" shift register. Data words are thus entered in series, the individual bits of the word passed through corresponding stages of the "parallel" shift registers and read out in series from the output shift register for recirculating. A plurality of such loops can be combined, the input and output data nevertheless being in serial form.

Because in such an arrangement the data is input and output in serial form, initialising or testing the entire memory array can take considerable time. It is known to use direct parallel accessing of the individual loops, but at the expense of requiring a higher number of inputs and outputs.

The invention overcomes this problem by the provision of a shift register having a number of cells equal in number to the number of memory elements, each cell being connectable to a respective memory element for the simultaneous reading and writing of data into or out of the memory elements in parallel, the data being clocked into and shifted through the cells of the shift register in the time interval between successive clocking steps of the memory elements.

4. It is common ground that the closest prior art to the invention as now claimed is D1. This document discloses a memory array including a plurality of recirculating memory elements in the form of recirculating memory shift registers 10 clocked by means of a clock 16. Although not explicitly stated in the document, the skilled man would understand from the presence of only a single clock line from the clock 16 to each of the shift registers 10 that the latter are clocked in synchronism, so that the corresponding bits recirculate in their respective loops with the same time phase. A buffer shift register 12 serves for the transfer of data into and out of the memory shift registers.

The construction and operation of buffer shift register 12 are not explained, movement of information into and out of this register being said to be twice as rapid as movement of information within the memory shift registers 10. A common data input and output line is used which, together with the presence of two arrows on the box of the buffer shift register, suggests that in like manner to the memory shift registers this is also a recirculating shift register. The document does not say whether each recirculating memory shift register has a single corresponding cell in the buffer shift register so that,

in the example shown in D1, there are four cells corresponding to the four recirculating memory shift registers. It seems however that each memory shift register corresponds to a single cell of the buffer shift register. Nothing is said of the operation of the input/output circuits 14 which connect the memory shift registers to the buffer shift register.

It is difficult to see how the device operates. The Examining Division considered two possible modes of operation, a "random access" mode in which a particular address is selected and a "sequential access" mode in which sequential addresses are selected. It is assumed that by "address" is meant a corresponding position of all the recirculating shift registers, so that the data word contained in these positions can be transferred to the buffer shift register and shifted out. By the inverse process a data word can be shifted in.

Dealing first with the "random access" mode, it is apparent that in any such mode the delays are primarily caused by stepping the recirculating memory shift registers until the desired address is found; in an arrangement with more than a handful of addresses the input/output shift times are small in comparison, so that the skilled man desiring an increase in overall speed is led to increase the speed not of the buffer register but of the memory registers.

It is not clear that a "sequential access" mode was ever envisaged for the device of D1. After the initial movement of data from the memory shift registers to the buffer shift register, no further such movement can take place until all the data has been read out of the buffer shift register. Unless during this time clocking of the memory shift registers is stopped, no consecutive data can then

be read out until the memory shift registers have recirculated to the bit immediately following the bit read out. Such an arrangement would be inordinately slow.

5. It therefore seems that D1 is not a document which the skilled man would consider seriously if he desired to improve the data transfer rate of a memory array having so-called "sequential access". Only with the benefit of hindsight is it obvious that by increasing the clock rate of the buffer shift register its contents can be read out between the clock pulses of the memory shift registers. The appreciation that this can be done through all the cells of the buffer shift register in the time interval between successive clocking steps of the memory shift registers could not be derived by the skilled man from the disclosure of D1 without the exercise of invention. The subject-matter of Claim 1 accordingly involves an inventive step having regard to the disclosure of D1.

6. Nor does the Board consider that the skilled man, starting out from the disclosure of D2, would be led to construct an arrangement falling within the scope of Claim 1. Figure 6b of D2 shows a "SPS" CCD loop memory. The clock rate of the input/output registers is M times higher than that of the memory registers so that between clock pulses in the memory registers an entire data word can be read into and out of the input/output registers. The entire arrangement constitutes a recirculating memory element, the output being connected back to the circuit input. The memory elements themselves are not recirculating, this function being provided by the connection between the input and output shift registers. There is no good reason why the skilled man should modify this known arrangement to provide recirculating memory elements in place of the memory shift registers. An array including a plurality of recirculating memory elements is

indeed known from Figure 9 of D2, but in the context of a quasi-random access memory in which the individually stored bits are called up as required.

Finally, the skilled man, interpreting D1 in the light of the disclosure of D2, would not be led to construct an arrangement falling within the scope of Claim 1. The Figure 9 arrangement of D2 would lead the skilled man to replace the buffer shift register by a logic circuit to enable random access to one of the memory shift registers. The Figure 6b circuit would be adopted by the skilled man as a suitable memory shift register arrangement; there is nothing in D2 which would lead him to see an analogy between on the one hand the two different clock rates used for the buffer and memory shift registers in D1 and on the other hand the clock rates of the series and parallel shift registers of Figure 6b of D2. Only with the benefit of hindsight is it obvious that such an analogy exists.

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent on the basis of the Appellant's request (paragraph VI. above), with the proviso that on page 2 of the description the reference numbers have to be deleted.

The Registrar: The Chairman:

M. Beer P.K.J. van den Berg