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Veröffentlichung im Amtsblatt	Ja/Nein
Publication in the Official Journal	Yes/No
Publication au Journal Officiel	Oui/Non

Aktenzeichen / Case Number / N° du recours : T 543/88 - 3.5.1

Anmeldenummer / Filing No / N° de la demande : 83 307 551.8

Veröffentlichungs-Nr. / Publication No / N° de la publication : 0 114 475

Bezeichnung der Erfindung:
Title of invention:
Titre de l'invention : Improvements in or relating to sample-and-hold circuits.

Klassifikation / Classification / Classement : G11C 27/02

ENTSCHEIDUNG / DECISION

vom / of / du 24 August 1989

Anmelder / Applicant / Demandeur : Western Electric Company

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Articles 56, 84 EPC

Schlagwort / Keyword / Mot clé : "Clarity of Claim and support by the description" - "Inventive step (yes)"

Leitsatz / Headnote / Sommaire

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Case Number : T 543/188 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 24 August 1989

Appellant : Western Electric Company, Incorporated
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Berkeley Heights
New Jersey 07922 - 2727 (US)

Representative : Buckley, Christopher Simon Thirsk et al,
Western Electric Company Limited
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Decision under appeal : Decision of Examining Division 067 of the European Patent Office dated 24 June 1988 refusing European patent application No. 83 307 551.8 pursuant to Article 97(1) EPC

Composition of the Board :

Chairman : P.K.J. van den Berg
Members : W. Riewald
E. Persson

Summary of Facts and Submissions

I. European patent application No. 83 307 551.8, claiming priority of 20 December 1982, filed on 12 December 1983 and published on 1 August 1984 under No. 0 114 475, was refused by a decision of the Examining Division 067 dated 24 June 1988.

The decision was based on Claims 1 to 4, received on 2 November 1987 with a letter dated 28 October 1987.

The reason given for the refusal was that the independent claim did not comply with the requirements of Article 84 EPC since it was not clear because essential features were missing.

In respect of inventive step, the Examining Division had indicated that grant could be envisaged provided the claims were clarified. Suggestions to this effect were made. The Examining Division had come to this conclusion by taking into account the following pertinent prior art documents:

D1: "Modern Electronic Circuits Reference Manual" McGraw-Hill Book Company, 1980, page 886;

D2: Patents Abstracts of Japan, Vol. 6, No. 59 (P-110) [937] April 16, 1982; & JP-A-56-169 291.

II. On 17 August 1988, the Appellant lodged an appeal against this decision. The appeal fee had been paid on 15 August 1988. Together with a Statement of Grounds, received on 21 October 1988, the Appellant filed two different versions of Claims 1 to 4, designated as "SET A" and "SET B" respectively, as auxiliary requests.

The Appellant, however, challenged the Examining Division's view in respect of the question concerning the clarity of Claim 1 and made the said auxiliary requests "without prejudice to the claims at present on file". This must be interpreted as a main request to grant a patent on the basis of the same application documents as recited in the impugned decision of the Examining Division.

III. In a communication, dated 20 January 1989, the Rapporteur was prepared only to follow the Appellant's arguments to some extent. He suggested to pursue the application on the basis of the claims designated "SET B" with some amendments regarded necessary in view of Article 84 EPC.

IV. The Appellant filed with letter of 15 March 1989, received 20 March 1989, a new set of Claims 1 to 4 to replace the former "Set B", but requested the revision of the application in the light of the submissions already made in an earlier application (EP-A-107 337) and in the present proceedings, since the Applicants still felt that their contribution to the art justified a comparably extensive claim.

Consequently, the Appellant's request to grant a patent has to be divided up into one main request and two auxiliary requests:

IV(a) As the main request, the Appellant maintains Claims 1 to 4, filed on 2 November 1987 together with adapted parts of the description.

IV(b) The first auxiliary request is based on "SET A" of Claims 1 to 4, filed on 21 October 1988 together with a further adapted part of the description.

IV(c) The second auxiliary request is based on the following application documents:

- description, pages 1, 2a, 4, 5, 7, 8 received on 2 November 1987 with letter dated 28 October 1987;
  page 2, received with the statement of grounds filed 21 October 1988;
  pages 3, 6 and 9 as published;

- Claims 1 to 4, filed with letter of 15 March 1989;

- drawings, sheet 1/2 as published;
  sheet 2/2 filed with letter of 28 October 1987.

V. Claim 1 of the main request reads as follows:

"1. A sample-and-hold circuit including a sampling switch (30) connected between a signal input and an input of a buffer (42), the buffer including an enhancement mode transistor (46) having a gate serving as the input of the buffer and its drain-to-source conduction path connected to bias current means (47), a holding capacitor (32) connected at a first side to the input of the buffer and at a second side to a reference potential, and feedback means (52,54,24) connected between the output of the buffer and an input of an amplifier, and CHARACTERISED IN THAT there is provided a correction switch (34) connected at its first side to the output of the amplifier, and a correction holding capacitor (36) connected at its first side to a reference potential and at its second side to the second side of the correction switch, and the buffer includes means (44) coupling the second side of the correction switch (34) to the drain of the enhancement mode transistor (46)."

VI. Claim 1 of the first auxiliary request reads as follows:

"1. A sample-and-hold circuit including a sampling switch (30) connected between a signal input and an input of a buffer (42), the buffer including an enhancement mode transistor (46) having a gate serving as the input of the buffer and its drain-to-source conduction path connected to bias current means (47), a holding capacitor (32) connected at a first side to the input of the buffer and at a second side to a reference potential, and feedback means (52,54,24) connected between the output of the buffer and an input of an amplifier, and characterised in that there is provided means for providing a signal for correcting switching charge feedthrough error on the holding capacitor which occurs when the sampling switch is opened, the providing means including a correction switch (34) connected at its first side to the output of the amplifier, and a correction holding capacitor (36) connected at its first side to a reference potential and at its second side to the second side of the correction switch, and the buffer includes means (44) coupling the second side of the correction switch (34) to the drain of the enhancement mode transistor (46)."

VII. Claim 1 of the second auxiliary request reads as follows:

"1. A sample-and-hold circuit including a sampling switch (30) connected between a signal input and an input of a buffer (42), the buffer including an enhancement mode transistor (46) having a gate serving as the input of the buffer and its drain-to-source conduction path connected to bias current means (47), a holding capacitor (32) connected at a first side to the input of the buffer and at a second side to a reference potential, and feedback means (52,54,24) connected between the output of the

buffer and an input of an amplifier, and characterized in that there is provided means for correcting switching charge feedthrough error on the holding capacitor which occurs when the sampling switch is opened, the providing means including a correction switch (34) connected at its first side to the output of the amplifier, and a correction holding capacitor (36) connected at its first side to a reference potential and at its second side to the second side of the correction switch, and the buffer includes means (44) for coupling a correction signal from the second side of the correction holding capacitor (36) to the holding capacitor (32) via the gate-to-drain capacitance (56) of the enhancement mode transistor (46) during an interval between the opening of the sampling switch (30) and the opening of the correction switch (34)."

Reasons for the Decision

1. The appeal complies with Articles 106-108 and Rule 64 EPC and is admissible.

2. Novelty

The different versions of Claim 1 have identical pre-characterising portions which represent prior art as disclosed in document D1.

The lower diagram of D1, page 886, shows a sample-and-hold circuit including a sampling switch Q_1 connected between a signal input and an input of a buffer. The buffer includes an enhancement mode transistor Q_2 having a gate serving as the input of the buffer. The drain-to-source conduction path of the buffer transistor is connected to a 30K resistor as a bias current means. A

holding capacitor (.0047) is connected at a first side to the input of the buffer and at a second side to a reference potential (ground). A feedback connection is provided between the output of the buffer and an input of an amplifier IC_1.

Claim 1 of the main request differs from this prior art by the additional provision of a secondary sample-and-hold circuit comprising a correction switch and a correction holding capacitor connected to the output of the amplifier and to a reference potential just in the same way as the sampling switch and the holding capacitor of the known circuit. However, whereas the second side (i.e. the side which is not connected to the signal input) of the sampling switch is connected to the gate of the buffer transistor, Claim 1 of the main request specifies that the second side of the correction switch is coupled to the drain of the enhancement mode transistor. The sample-and-hold circuit of document D2 differs from that of the present application already in respect of the precharacterising portion since it does not comprise a feedback arrangement.

The description of the present application acknowledges on page 4, first paragraph, as prior art the content of an earlier European patent application published under No. EP-A-107 337 after the filing date of the present application and disclosing the dual feedback sample-and-hold principle with a primary sample-and-hold circuit and a secondary sample-and-hold circuit, the secondary circuit providing the primary circuit with voltage error correction. The subject-matter of all three versions of Claim 1 in the present application differ from this document (that represents prior art under Article 54(3) EPC) by details concerning the buffer including an enhancement mode transistor.

The subject-matter of Claim 1 in all three versions is thus to be considered novel.

3. It has, however, to be examined whether the different versions of Claim 1 meet the requirements of clarity and support by the description (Article 84 EPC).

The description deals on page 1, line 14 to page 2, line 1 with a so-called fixed pattern noise, which problem arises from a switching charge feedthrough error on the holding capacitor following the operation of the sampling switch from "ON" condition to "OFF" condition.

Claim 1 of the first auxiliary request differs from Claim 1 of the main request in that it additionally specifies the purpose of the correction arrangement, viz. to provide a signal for correcting the said switching charge feedthrough error. However, as set forth below, neither Claim 1 of the main request, nor Claim 1 of the first auxiliary request can be regarded as sufficiently clear in respect of the necessary means to ensure this desired function.

The description deals, furthermore, on page 2, lines 2 to 11 with the power "supply rejection problem", which arises from a parasitic coupling of power supply noise to the holding capacitor via the drain-to-gate capacitance of the enhancement mode transistor. Also in respect of a solution to this problem, Claim 1 in its version according to the main request and first auxiliary request cannot be regarded as sufficiently clear.

The following details can be understood from the description as relevant for the solution of the said two problems in the context of the present disclosure:

- The second side of the correction switch need not be directly coupled to the drain of the enhancement mode transistor. The embodiment of Figure 1 shows, in contrast, that the correction signal from the second side of the correction holding capacitor is coupled to the said drain through a depletion mode transistor (44), which serves as a unity gain buffer to the source node (48) of transistor (44) and consequently also to the drain of the enhancement mode transistor (46), (see page 7, lines 1 to 3). In order to avoid any inconsistency between claim and description, it is therefore more correct to specify that it is the correction signal that is coupled to the drain of the enhancement mode transistor.

- The present invention is based on the principle to correct the charge feedthrough error introduced by the opening of the sampling switch by subsequently effecting a feedback control of the output voltage by means of the said secondary sample-and-hold circuit. This requires that there is a time interval between the opening of the sampling switch and the opening of the correction switch during which the correction switch is closed (see page 6, lines 16 to 34).

  This essential timing condition is neither specified in Claim 1 according to the main request nor in Claim 1 of the first auxiliary request

- The correction signal is coupled to the holding capacitor via the gate-to-drain capacitance of the enhancement mode transistor.

The gate-to-drain capacitance has the effect of attenuating the coupling of the correction capacitor to the holding capacitor, thereby correspondingly attenuating the effect of the charge feedthrough error generated by the opening of the correction switch in the secondary sample-and-hold circuit (cf. page 6, lines 8 to 34). A similar attenuation effect is attained by the said gate-to-drain capacitance for the parasitic coupling of noise in the power supply rail (page 7, lines 5 to 14).

Consequently, a suitable gate-to-drain capacitance is necessary for carrying out the invention. However, this gate-to-drain capacitance is neither specified in Claim 1 according to the main request nor in Claim 1 of the first auxiliary request.

4. Since, as set out above, the versions of Claim 1 according to the main request and to the first auxiliary request do not clearly specify all the essential features of the invention, these claims are not allowable with regard to Article 84 EPC (cf. decision T 32/82, OJ EPO 8/1984, 354-356, in particular No. 15 of the Reasons).

The Appellant's submission that, even if essential features were missing, lack of clarity is not a logical or necessary consequence, and that the test for clarity of a claim is whether the scope of protection is clear, cannot be accepted. A necessary condition of patentability is that the scope of protection is clearly restricted to what can be regarded as the invention (in the sense of Article 52(1) EPC) as disclosed in the description (according to Article 83 EPC). That means that a speculative broadening of the scope of protection over that what has been really disclosed as the invention

cannot be allowed (the claim must "be supported by the description", Article 84 EPC).

5. There are no objections under Article 84 to Claim 1 according to the second auxiliary request.

All the features discussed above, and which concern the coupling of the correction signal to the holding capacitor via the said gate-to-drain capacitance and the necessary timing for the sampling switch and the correction switch, have been incorporated in the last six lines of Claim 1 of the second auxiliary request.

The Board is satisfied that it is not necessary to specify in Claim 1 that the input of the sampling switch (of the primary sample-and-hold circuit) is connected to the output of the amplifier (in contrast to the suggestion in point 4.2 of the Rapporteur's communication of 20 January 1989).

The Appellant's broader wording is backed by the originally filed Claim 1. Therefore, no objection under Article 123(2) arises.

The Board agrees to the said broader wording of Claim 1, also in respect of Article 84 for the following reasons: The present invention realises a concept in which, in a first step the holding capacitor of a primary sample-and-hold circuit is to be charged to a voltage approximately equal to the input voltage.

Remaining small differences to the input voltage can be reduced in a second step, by the secondary sample-and-hold circuit which has to correct the error voltage on the holding capacitor. The amplifier and feedback arrangement as well as the coupling of the correction signal via the

said gate-to-drain capacitance are necessary means for this function. However, it is clear that the first step, i.e. the charging of the holding capacitor of the primary sample-and-hold circuit to only approximately the input voltage, can already be effected by a sample-and-hold circuit in its simpler form, i.e. without an amplifier and feedback arrangement. Such simpler sample-and-hold circuits belong to the background knowledge in this technical field (see, for instance, document D2). The Board is therefore satisfied that the connection of the sampling switch of the primary sample-and-hold circuit directly to the input signal node is an embodiment which the skilled person might readily envisage with the knowledge of the general teaching of the present application and which should not be excluded by a restricted wording of Claim 1.

Since it is now clear that the essential features of the claimed invention concern the details of the sample-and-hold arrangement on the input side of the buffer whereas the buffer output may be modified (e.g. by additional circuits as suggested in the Appellant's reply of 15 March 1989, page 2, last paragraph), the Board also refrains from requiring a closer specification of the buffer output.

6. Inventive step

It remains to examine whether the subject-matter of Claim 1 of the second auxiliary request is based on an inventive step.

Document D1, from which the present invention starts, comprises only a single sample-and-hold circuit and does not disclose any means of correcting a switching charge feedthrough error.

Document D2 discloses such means, but comprises also only a single sample-and-hold circuit. The switching charge feedthrough effect is compensated for by a pulse via a capacitor which is series-connected to the holding capacitor. But, this pulse is not generated in a secondary sample-and-hold circuit, nor is there provision made for a feedback arrangement. Therefore, the Board is satisfied that the Examining Division's finding in its first communication (dated 3 July 1987) is correct, according to which a modification of the sample-and-hold circuit of D1 by incorporating the teaching of D2 would not render the subject-matter of the application obvious.

The content of EP-A-107 337, which as set out in Section 2 above, is not prejudicial to novelty of the subject-matter claimed, is not to be considered in deciding whether there is an inventive step (Article 56, second phrase).

7. Claim 1 of the second auxiliary request is thus allowable. Claims 2 to 4 are dependent claims specifying particular embodiments and are also allowable.

There are no objections to the description which has been brought into accordance with the amended scope of protection.

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.

2. The main request and the first auxiliary request for granting a patent are refused.

3. The case is remitted to the first instance with the order to grant a European patent on the basis of the second auxiliary request with the documents recited in Section IV(c) of this decision.

The Registrar: The Chairman:

S. Fabiani P.K.J. van den Berg