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Bezeichnung der Erfindung:
Title of invention:
Titre de l'invention : CMIS circuit device

Klassifikation / Classification / Classement : G11C 8/00

ENTSCHEIDUNG / DECISION

vom / of / du 26 April 1990

Anmelder / Applicant / Demandeur : Fujitsu Limited

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Article 56

Schlagwort / Keyword / Mot clé : "inventive step - no"

Leitsatz / Headnote / Sommaire

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Case Number : T 265/89 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 26 April 1990

Appellant : Fijitsu Limited
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Decision under appeal : Decision of Examining Division 067 of the European Patent Office dated 24 November 1988 refusing European patent application No. 83 056 677.3 pursuant to Article 97(1) EPC

Composition of the Board :

Chairman : P.K.J. van den Berg
Members : W.J.L. Wheeler
R.E. Persson

Summary of Facts and Submissions

I. Appellant's European patent application No. 83 305 677.3, filed on 23 September 1983, claiming priority from a previous application in Japan dated 28 September 1982, was refused by a decision of the Examining Division dated 24 November 1988. That decision was taken on the basis of Claim 1 filed with a letter dated 15 July 1988 and Claims 2 to 9 as originally filed.

II. The reason given for the refusal was that the subject-matter of the claims did not involve an inventive step, having regard to common general knowledge and the following prior art document:

D1: EP-A-0 031 672 (which was published in July 1981).

III. On 24 January 1989 the Appellant filed a notice of appeal against that decision. The appeal fee was paid on 25 January 1989. The statement of grounds was filed on 30 March 1989, together with new Claims 1 to 7 to replace all the previous claims.

IV. Claim 1 is now worded as follows:

"1. A CMIS integrated circuit device comprising a first power source line (Vcc); a second power source line; a CMIS inverter (Q20,Q21) having an input node, an output node, a first power supply node connected to the first power source line, and a second power supply node connected to the second power source line; and a first MIS transistor (Q_{19}) of a first conductivity type connected between one of the first and second power supply nodes and the adjacent power source line, characterised in that the device comprises a chip selection circuit, wherein the input node of the CMIS inverter receives a first external

chip-select signal (CS_2) which designates a chip select state in a first logical level and wherein a gate of the first MIS transistor of the first conductivity type receives a second external chip-select signal ($\overline{CS}_1$) which designates the chip select state in a second logical level complementary to the first logical level; and in that the device further comprises a logic gate (Q23, Q24, Q25, Q26) having an input node connected to the output node of the CMIS inverter (Q20, Q21) and an output node for outputting an internal chip-select signal (CS) to control the CMIS integrated circuit device, the logic gate including second and third MIS transistors (Q23, Q24) of the first conductivity type connected in series between the one power source line (Vcc) and the output node of the logic gate, first and second MIS transistors (Q25, Q26) of the second conductivity type, opposite to the first conductivity type, connected in parallel between the output node of the logic gate and the other power source line, gates of the second MIS transistor (Q23) of the first conductivity type and the first MIS transistor (Q25) of the second conductivity type being connected to the input node of the logic gate, and gates of the third MIS transistor of the first conductivity type (Q24) and the second MIS transistor (Q26) of the second conductivity type receiving the second external chip-select signal ($\overline{CS}_1$)."

Claim 2 relates to a CMIS integrated circuit device comprising a plurality of IC chips and a corresponding plurality of chip selection circuits, each chip selection circuit having all the features specified in Claim 1.

Claim 3 is worded as follows:

"3. A CMIS integrated circuit device according to Claim 1 or Claim 2, wherein the or each chip selection circuit further comprises a fourth MIS transistor of the first

conductivity type (Q32) connected between the one of the first and second power source nodes of the CMIS inverter and the adjacent power source line and having a gate receiving a third external chip-select signal ($\overline{CS}_3$) which designates the chip select state in the second logical level; and wherein the logic gate further comprises a fourth MIS transistor (Q34) of the second conductivity type connected in parallel with the first and the second MIS transistors (Q25, Q26) of the second conductivity type, the gate of the fourth MIS transistor (Q34) of the second conductivity type receiving the third external chip-select signal ($\overline{CS}_3$)."

Claims 4 to 7 are dependent upon any of Claims 1 to 3.

V. In a communication of the Board pursuant to Article 11(2) of the Rules of Procedure of the Boards of Appeal, the Board pointed out that the closest prior art appeared to be that acknowledged in the present application with reference to Figure 6, that it appeared from the discussion of the prior art in the application that the problem to be solved had already been recognised, and that the solution claimed did not appear to involve an inventive step in the light of document D1.

VI. Oral proceedings were held on 26 April 1990. The Appellant explained the line of development which had led, via the prior art devices shown in Figures 3 to 6 of the present application, to the presently claimed device. Although the devisers of the circuit shown in Figure 6 were trying to provide a battery back-up condition in which no current flowed from the battery when either one of two external chip-select signals having chip-select states of opposite polarity was in the chip-deselect state, irrespective of the level of the other chip-select signal, they had not been completely successful, since current could flow through the CMIS inverter (Q20, Q21) if the first chip-

select signal (CS_2) was not in the chip-deselect state (0V). This showed it could not have been obvious to provide an extra transistor connected between one of the power supply nodes of the inverter (Q20, Q21) and the adjacent power source line, or the devisers of the Figure 6 circuit would have done it. The document D1 did not concern a chip-select circuit but an address buffer circuit, analogous to the input circuit (IPC) shown in Figure 6 of the present application.

The Appellant further submitted that the transistor (Q33) shown in Figure 10 of the application had accidentally been omitted from dependent Claim 3. He argued that the subject-matter of that claim, amended to include the transistor Q33, would not be obvious from the prior art.

VII. The Appellant requests that the decision under appeal be set aside and a patent granted on the basis of Claims 1 to 7 as filed with the statement of grounds of appeal, or, as an auxiliary request, on the basis of Claim 3, possibly amended to specify the transistor Q33.

Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is, therefore, admissible.

2. The Appellant acknowledges that the closest prior art to the subject-matter now claimed is the circuit shown in Figure 6 of the present application. That circuit was designed to provide chip-selection when the chip-select signals (CS_2, $\overline{CS_1}$) have chip-select states of opposite polarity, and to provide battery back-up when either one of those chip-select signals is in its chip-deselect state, irrespective of the level of the other chip-select signal. The design goal was not, however, fully achieved,

because current can flow through the inverter (Q20, Q21) when the first chip-select signal (CS_2) is not in its chip-deselect state (0V).

3. The CMIS integrated circuit device according to Claim 1 differs from the closest prior art circuit only in that an extra MIS transistor (Q19) of the first conductivity type is provided, connected between one of the first and second power supply nodes of the CMIS inverter (Q20, Q21) and the adjacent power source line, the gate of this extra transistor (Q19) receiving the second external chip-select signal ($\overline{CS}_1$). When the transistor (Q19) is turned off by the second chip-select signal being in its chip-deselect state, it blocks the current path through the inverter (Q20, Q21) irrespective of the level of the first chip-select signal (CS_2). This overcomes the defect in the prior art circuit noted in paragraph 2 above.

4. In the opinion of the Board, a skilled person starting from the prior art circuit shown in Figure 6 of the present application (and not from one of the earlier circuits shown in Figures 3 to 5, as the devisers of the Figure 6 circuit had to do) could be expected to identify the flaw in that circuit and to try to eliminate it. In particular, he could be expected to realise that the current path through the inverter (Q20, Q21) should be blocked whenever the second chip-select signal ($\overline{CS}_1$) is in its chip-deselect state, as such a measure would obviously ensure that the desired battery back-up condition is obtained, irrespective of the level of the first chip-select signal (CS_2).

5. Document D1 discloses with reference to its Figure 6 a circuit comprising a CMIS inverter (11, 12) which is placed in a battery back-up condition by a signal ($\overline{\Phi*}$) applied to the gate of a MIS transistor (14) connected between one of the power supply nodes of a CMIS inverter

(11, 12) and a power source line (V_D). D1 indicates that without this transistor (14) a current would flow through the CMIS inverter (11, 12) unless the level of the input signal (A_{in}) to the inverter is controlled to remain within certain specified ranges. The MIS transistor (14) blocks current through the inverter under control of the signal ($\overline{\Phi*}$), independently of the level of the input signal (A_{in}) to the inverter, thereby reducing power consumption (see D1: Claim 1, pages 5 to 8 and 10 and Figures 4 to 6).

6. While it is true that D1 relates to an address buffer circuit, as pointed out by the Appellant, in the opinion of the Board, the skilled person would nevertheless obtain from D1 a teaching which is not limited to address buffer circuits. In particular, D1 discusses in detail the circumstances which result in current flowing through a CMIS inverter. The skilled person would therefore recognise that the solution suggested in D1 can be applied in general to any circuit when it is desired to block current flow through a CMIS inverter without controlling the input signal to the inverter.

7. For these reasons the Board considers that the skilled person looking for a solution to the problem identified in paragraph 2 above would consider applying the solution suggested in document D1. He would thus be led to provide an extra MIS transistor in series with the inverter (Q20, Q21). He would also be led to arrange for the gate of this extra transistor to receive the second chip-select signal ($\overline{CS_1}$), since it is required that the current path through the inverter be blocked under control of this signal. Proceeding in this way, the skilled person would arrive in an obvious manner at a device according to Claim 1. Consequently Claim 1 cannot be allowed as its subject-matter does not involve an inventive step.

8. As acknowledged in the present application it is known in the prior art to select a particular IC chip among a plurality of IC chips by means of chip-select signals, the unselected chips assuming a battery back-condition. In the opinion of the Board, it would be obvious to the skilled person to put the chip selection circuit defined in Claim 1 on each of the chips to be selected, thereby arriving at the subject-matter of Claim 2, which thus lacks inventive step.

9. Claim 3 relates to the case in which three chip-select signals are used. The transistors (Q32, Q34), whose gates receive the third chip-select signal (CS_3), are connected in the same way as the transistors (Q19 and Q26) whose gates receive the second chip-select signal (CS_1). The transistor Q33, which is shown on Figure 10 of the present application but not mentioned in Claim 3, serves the same purpose in respect of the third chip-select signal as the transistor Q24 does in respect of the second chip-select signal. While it is true, as the Appellant pointed out, that no prior art document on file discloses the use of three chip-select signals, the provision of three (or more) selectable chips in an apparatus is, to the knowledge of the Board, nothing new in itself. In the opinion of the Board, the provision of a third chip-select signal would obviously be desirable in such a situation. The features specified in Claim 3, as it stands or amended as requested by the Appellant to include the transistor Q33, amount to no more than a straightforward duplication for the third chip-select signal of the measures used to process the second chip-select signal, which measures have already been shown to be obvious.

10. The Board has therefore come to the conclusion that none of the Claims 1 to 3 submitted by the Appellant can be allowed, because their subject-matter does not involve an inventive step within the meaning of Article 56 EPC.

Consequently, all the Appellant's requests have to be rejected.

Order

For these reasons, it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

P. Martorana P.K.J. van den Berg