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Aktenzeichen / Case Number / N^o du recours : T 309/89 - 3.4.1

Anmeldenummer / Filing No / N^o de la demande : 82 901 672.4

Veröffentlichungs-Nr. / Publication No / N^o de la publication : 77 813

Bezeichnung der Erfindung: Low resistivity composite metallization for
Title of invention: semiconductor devices and method therefor
Titre de l'invention :

Klassifikation / Classification / Classement : H01L 29/04, H01L 23/48,
H01L 29/46, H01L 29/54

ENTSCHEIDUNG / DECISION

vom / of / du 20 August 1990

Anmelder / Applicant / Demandeur :

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

MOTOROLA, INC.

Einsprechender / Opponent / Opposant :

Deutsche ITT Industries GmbH

Stichwort / Headword / Référence :

EPO / EPC / CBE Article 56

Schlagwort / Keyword / Mot clé :

"Inventive step (no)"

Leitsatz / Headnote / Sommaire

Europäisches
Patentamt

Beschwerdekammern

European Patent
Office

Boards of Appeal

Office européen
des brevets

Chambres de recours



Case Number : T 309/89 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 20 August 1990

Appellant : Deutsche ITT Industries GmbH
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Representative : Dr. Reichel
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Decision under appeal : Decision of Opposition Division of the European
Patent Office dated 15 March 1989 rejecting
the opposition filed against European patent
No. 77 813 pursuant to Article 102(2) EPC.

Composition of the Board :

Chairman : K. Lederer
Members : Y.J.F. van Henden
L. Mancini

Summary of Facts and Submissions

I. European patent No. 0 077 813 was granted on European patent application No. 82 901 672.4.

II. Claim 1 as granted reads

"1. A semiconductor device having a composite metallization structure comprising:

a first layer of conductive intermetallic material (44; 69) formed on a portion of said device;

a second layer of protective and conductive intermetallic material (49; 70) different from said first layer, said second layer covering said first layer for providing a protective cap and facilitating electrical connection to said first layer; and

wherein the combination of said first and second layer forms said composite metallization."

The Claims 2-6 are dependent on Claim 1. Claims 7 to 12 are all independent process claims.

III. An opposition was filed against the European patent by the Appellant who requested said patent to be revoked in its entirety.

The Appellant cited inter alia the documents:

D1: US-A-4 227 944

- D2: IEEE Transactions on Electron Devices, Vol. ED-26, No. 4 (April 1979), pages 369-371, B.L. Crowder et al. "1 μ m MOSFET VLSI technology: Part VII - Metal silicide interconnection technology - A future perspective"
- D4: Journal of vacuum science & technology, Vol. 17, No. 4 (July/August 1980), pages 775-792, S.P. Murarka "Refractory silicides for integrated circuits"
- D7: Applied Physics Letters, Vol. 36, No. 6 (March 1980), pages 456-458, M. Wittmer "TiN and TaN as diffusion barriers in metallizations to silicon semiconductor devices"
- D8: EP-A-0 000 317

and argued that the subject-matter of the granted claims was not inventive in view of this prior art.

- IV. The Opposition Division rejected the opposition.
- V. An appeal was lodged against this decision.
- VI. In a communication pursuant to Article 110(2) EPC, the Rapporteur of the Board expressed his provisional opinion with consideration to the state of the art revealed by documents (D1, D2, D4, D7, D8).
- VII. The Respondent (Proprietor of the patent) replied on 28 June 1990 and submitted new Claims 1-12.
- VIII. Claim 1 as submitted on 28 June 1990 differs from the granted version in that the mention "and extending on top and to the sides thereof" has been inserted between "covering said first layer" and "for providing a protective cap" in the second clause, and in that "forms"

has been replaced by "form" in the last clause. The Claims 2-6 appended to said Claim 1 are identical to the corresponding ones of the patent in suit.

The Claims 7-12 received on 28 June 1990 are process claims corresponding to Claims 7-12 as granted without any substantial amendment.

- IX. The Appellant requested the decision of the Opposition Division to be set aside and the patent in suit to be revoked. The Appellant also requested oral proceedings to be held if the Board were to find against him.

From the last two paragraphs of the Respondent's reply of 28 June 1990, the Board infers that the Respondent requests the appeal to be dismissed and the patent maintained unamended, and, subsidiarily, that he requests maintenance of the patent on the basis of the new Claims 1-12 submitted with said reply.

- X. The Appellant substantially argues as follows:

The argumentation of the Opposition Division relies on the fact that the cited references do not reveal the claimed arrangement of layers, and that document (D2) would insist upon the oxidisability of metal silicides and thus deter the skilled person from using them. It is, however, pointed out in section I of (D2) that the use of such silicides is advisable because of their resistance to oxidisation and, in section III, that an oxide film protects them against any further attack. Furthermore, it is known from (D1) that said silicides provide low electrical resistance paths.

It is true that metal silicides do not oppose silicon diffusion. Nevertheless, from (D7), the skilled person

learns that metal nitrides oppose said diffusion. The generality of this teaching is not affected by its disclosure in relation with a different arrangement, and the less so as the skilled person is, in the present case, a university graduate. Said person is thus able to combine the teachings of (D2) and (D7) to arrive at the invention without having to display any inventive talent. Likewise, the claimed processes do not involve an inventive step for they just comprise elementary steps that are widely known and performed while making multilayer devices.

XI. The Respondent substantially argues as follows:

It is not disputed that document (D7) teaches the use of TaN or TiN as a diffusion barrier to prevent outward migration of the underlying silicon in electrical contacts for semiconductor devices, nor that it describes a Si + Cr (forms CrSi₂) + TiN or TaN + Ni composite metallisation as solving the solderability problem of such contacts. However, there is no consideration in (D7) about the sides or edges of the underlying layers since what happens to said sides or edges is irrelevant to the above problem. Also, there is no consideration of a composite metallisation in which the solderable Ni layer is omitted.

As a matter of fact, none of the cited documents reveals or even suggests the idea of subjecting semiconductor devices to routine testing that would show up possible shortcomings of metallisations. The Respondent, whose concern is to avoid oxidation of the very sensitive silicide underlayer, has the merit of having recognised that sideways etching or oxidation of the base silicon or silicide would eventually damage, if not destroy, the composite metallisation. He also found that TiN and TaN

are both highly conductive electrically, that they prevent oxygen from attacking the underlying silicide, and that sideways etching or oxidation could be obviated by providing the upper oxidation barrier in the form of a cap which completely covers the underlying layers. The skilled person attempting to solve the Respondent's problem would indeed not have learnt such a disposition from (D1), for the latter, which describes a structure where a substantial portion of a silicide layer is converted to oxide, i.e. precisely the structure which the Respondent wishes to avoid, would be considered as irrelevant to said Respondent's problem. Having regard thereto, the reasoning set out in the Rapporteur's communication would be a classic hindsight interpretation of the references.

Reasons for the Decision

1. The appeal is admissible.
2. Novelty
 - 2.1 Document (D7) relates to semiconductor devices comprising metallisation structures - cf. title. It reveals inter alia that, if a substrate made of silicon and coated with a Cr/TaN/Ni metallisation is annealed for 10 mn at 500°C, the entire chromium layer reacts with silicon and that, besides chromium silicide formation, no other reaction takes place - see page 458, lines 9 to 18 of the left-hand column. It is further stated in (D7) that no alteration of a so called Ni signal is observed, which would be the case if some silicon would have diffused through the TaN layer and reacted with the top Ni layer - see page 458, lines 17 to 21 of the left-hand column.

Therefore, it goes without saying that, in the semiconductor device known from (D7), the chromium silicide layer is adjacent the substrate, hence that it is formed on a portion of the semiconductor device, and that the tantalum nitride layer covers the chromium silicide layer.

- 2.2 The use of chromium silicide for making the first layer and that of tantalum nitride for making the second layer is envisaged in the patent in suit - cf. Claims 2 and 3. It may thus not be denied that, in the semiconductor device known from (D7), the combination of the chromium silicide layer adjacent the substrate and tantalum nitride layer covering said chromium silicide layer forms a composite metallisation structure comprising layers of different intermetallic materials within the meaning of valid Claim 1.
- 2.3 Although the problem of developing very large scale integrated circuits with corresponding small contact areas is mentioned at the beginning of document (D7), no explicit reference to electrical connections of semiconductor devices can be found there. Nevertheless, it is stated on page 458 of said document, second paragraph of the right-hand column, that the Ni layer covering the tantalum nitride layer is provided for soldering the semiconductor device to a heat sink. Moreover, it is known that, in most apparatus comprising integrated circuits, the heat sink also forms the earth, which means that its connection to said circuits is an electrical one. Finally, it is also stated in the above-mentioned paragraph of page 458 that tantalum nitride has a low electrical resistivity, and that its adherence to silicides and metal layers is good. Therefore, in the semiconductor known from (D7), the layer of tantalum nitride is conductive and facilitates electrical connection to the first layer of conductive intermetallic material.

- 2.4 With regard to the preceding, and accepting the Respondent's interpretation of the word "cap", the subject-matter of Claim 1 according to either of the Respondent's requests distinguishes over the prior art known from (D7) in that no nickel top layer is provided, and in that the second layer of protective and conductive intermetallic material also extends to the sides of the first layer.
3. Inventive step
- 3.1 The Board shares the Appellant's view that the skilled person to be referred to while assessing inventiveness in the present case is a university graduate, i.e. a person understanding that the validity of information disclosed in a technical or scientific publication may well extend to a domain broader than the specific field said publication tackles. The Board furthermore takes the view that no skilled person attempting to solve a particular technical problem in his specific field of activity may be assumed not to be aware of other technical problems which are known to belong to said field of activity, and not to take said other problems into account while seeking a solution to said particular problems.
- 3.2 The Board now observes that document (D7) pertains to composite metallisations comprising a metal top layer and discloses a solution for preventing said top layer from being damaged by silicon diffusing through an underlying silicide layer. The author of (D7) had, therefore, no reason to take into consideration composite metallisations where no metal top layer is provided, nor to disclose details of their fabrication that were not directly

related to his concern. Nevertheless, any reader having received university education is able to understand that and, consequently, to investigate whether alternative arrangements are envisageable. Knowing that tantalum nitride has a good adherence to metals and a low electrical resistivity, said reader does not need to exert any inventive talent to abandon the provision of a metal top layer.

3.3 In the impugned decision, the Opposition Division took the view that the tantalum nitride layer of the device described in (D7) being provided for preventing silicon diffusion toward the top nickel layer, the skilled person would not envisage to omit the latter without omitting the nitride layer too. The Board, however, cannot share this view. The skilled person knows indeed that solder materials to be used here are metallic ones, thus liable to be damaged by silicon diffusion. Bearing this in mind, he readily understands that providing a barrier against silicon diffusion in the case of contacts with no metal top layer is not irrelevant.

3.4 The Board now observes that the reliability of integrated circuits, which are semiconductor devices of the kind contemplated in the patent in suit, must be very high. Such circuits are indeed essential parts of computers, i.e. apparatuses that are widely used for controlling industrial or commercial activities, in particular financial transactions. Therefore, it is excluded to sell integrated circuits without having previously subjected at least the prototypes thereof to all envisageable tests and controls, as well as to make such expensive prototypes without having previously investigated on the basis of theory the possible shortcomings of their design. This means that an effect such as undercutting, which is anyway widely known in the art, is not liable to escape the

attention of the skilled person carrying out routing tests in order to perfect the design of semiconductor devices. At this stage of the development, however, it becomes obvious to the skilled person that the simplest available solution to the problem is to make the upper layer extend not only on top but also to the sides of the underlying layer. This solution is indeed of general application in the field of integrated circuits and it may not be assumed that the skilled person would not be informed of its principle, since the latter is revealed by document (D1) - see the Figures 3D, 3E and related parts of the description.

Furthermore, the Respondent's arguments concerning the prevention of silicide oxidisation are not liable to invalidate the Board's reasoning. It appears indeed that, in any case, silicon diffusion towards the junction with co-operating elements, for instance soldered connexion wires or contacts of other devices, must be precluded. Thus, the avoidance of silicide oxidation rather is to be considered a bonus effect which cannot render inventive the obvious solution of another problem, here to avoid silicon diffusion.

- 3.5 With regard to the preceding, it appears that a skilled person analysing the teachings of document (D7) critically and bearing in mind his basic technical knowledge would, without having to display inventive talent, arrive at the subject-matter of Claim 1 according to either of the Respondent's requests.
4. Claim 1 according to either of the Respondent's requests lacking an inventive step, Article 56 in combination with Article 100(a) EPC prejudices the maintenance of the patent in suit with either of said claims. Therefore, according to Article 102(1) EPC, the patent has to be revoked as a whole.

5. Furthermore, the Board perceiving no patentable subject-matter in any of the dependent Claims 2-6 nor in any of the independent Claims 7-12, neither in their granted form, as already pointed out in the Board's communication, point 2.9 to point 7., nor in their amended form according to the Respondent's auxiliary request, there was no reason to give the Respondent a further opportunity to amend his patent.
6. The request for oral proceedings being contingent on the Board finding against the Appellant, which was not the case, holding such proceedings was not necessary.

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.
2. The patent is revoked.

The Registrar:

The Chairman:

M. Beer

K. Lederer