Europäisches Patentamt
Beschwerdekammern

European Patent Office
Boards of Appeal

Office européen des brevets
Chambres de recours

Veröffentlichung im Amtsblatt	Ja/Nein
Publication in the Official Journal	Yes/No
Publication au Journal Officiel	Oui/Non

Aktenzeichen / Case Number / N° du recours : T 471/89 - 3.5.1

Anmeldenummer / Filing No / N° de la demande : 83 401 825.1

Veröffentlichungs-Nr. / Publication No / N° de la publication : 0 104 120

Bezeichnung der Erfindung: Redundant columns for byte wide memories
Title of invention:
Titre de l'invention :

Klassifikation / Classification / Classement : G06F 11/20

ENTSCHEIDUNG / DECISION

vom / of / du 7 August 1990

Anmelder / Applicant / Demandeur : Fairchild Semiconductor Corporation

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Article 56

Schlagwort / Keyword / Mot clé : "Inventive step (no) - obvious modifications"

Leitsatz / Headnote / Sommaire

Europäisches Patentamt
Beschwerdekammern

European Patent Office
Boards of Appeal

Office européen des brevets
Chambres de recours

Case Number : T 471/89 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 7 August 1990

Appellant : Fairchild Semiconductor Corporation
10400 Ridgeview Court
P.O. Box 1500
Cupertino, California 95014
US

Representative : Sparing Röhl Henseler
Patentanwälte
European Patent Attorneys
Rethelstrasse 123
D-4000 Düsseldorf 1

Decision under appeal : Decision of Examining Division 065 of the European Patent Office dated 15 February 1989 refusing European patent application No. 83 401 825.1 pursuant to Article 97(1) EPC

Composition of the Board :

Chairman : P.K.J. van den Berg
Members : W.B. Oettinger
M. Lewenton

Summary of Facts and Submissions

I. European patent application No. 83 401 825.1 (publication No. 0 104 120) claiming a priority as from 20 September 1982 and filed on 20 September 1983, was refused by decision of Examining Division 2.2.01.065 dated 15 February 1989.

II. That decision was based on Claim 1 filed on 29 October 1988 and Claims 2-10 as originally filed on the ground that the subject-matter of these claims was not considered to involve an inventive step with respect to the prior art disclosed in the following documents:

D1: IBM Journal of Research & Development, Volume 24, No. 3, May 1980, pages 291-298, and

D2: IEEE Transactions on Electronic Devices, Volume ED-26, No. 6, June 1979, pages 853-860.

III. The Applicant lodged an Appeal against this decision on 11 April 1989 and paid the relative fee on the same day. On 15 June 1989, the Appellant filed a Statement of Grounds containing a subsidiary request for oral proceedings.

IV. In response to a Communication pursuant to Article 11(2) of the Rules of Procedure of the Boards of Appeal, the Appellant faxed on 6 July 1990 an amended version of Claim 1 and confirmed it on 7 July 1990.

V. In Oral Proceedings, held on 7 August 1990, the Appellant requested that the decision under appeal be set aside and the case be remitted to the first instance for further prosecution on the basis of a claim comprising the subject-matter of both Claim 1 as filed on 6 July 1990 and Claim 2 as originally filed.

Said Claims 1 and 2 read as follows (with two clerical errors corrected):

"1. Byte wide memory wherein each byte includes n bits, each bit includes m sense amplifiers (11), and each sense amplifier has associated with it p columns of memory cells, comprising a spare column of memory cells; an electrically conductive line (13); decoder means (T_D, 16) for switchably connecting the line (13) to the spare column; a first fusable connection (FSD1) between the spare column and the line (13); m per bit second fusable connections (FS, T, 14) for selectively connecting one of the m sense amplifiers (11) to the line; and p per sense amplifier third fusable connections (FD), each connected between a corresponding one of the p columns and the sense amplifier (11) associated with that column.

2. Memory as in Claim 1, characterized in that each of the m second fusable (FS) connections comprises:

switching means (T) connected between the line (13) and the sense amplifier (11); and

a fuse (FS) connected between a first potential source and the switching means to control the switching means."

VI. Essentially the Appellant submits the following arguments:

According to the appealed decision three steps would be necessary to arrive "directly" at the subject-matter of Claim 1 from the prior art disclosed in D1. However none of these steps is suggested in D1; rather they are all derived from the teaching provided by the present application.

Furthermore the Appellant does not consider that there is a "direct" connection between the prior art according to D1 and the claimed invention.

D1 teaches away from the invention as it states that redundant columns must have unique sense amplifiers (data latches). Where it refers to alternatives, it is not clear what modifications must be made.

Furthermore D1 does not disclose the features specified in Claim 2. By virtue of these features the defective column is clearly associated with one fuse, which has to be blown to repair the circuit. Thus the memory of the invention is easier to repair than the memory disclosed in D1.

Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is, therefore, admissible.

2. With respect to the originally filed Claim 1, present Claim 1 has been amended regarding the number of second and third fusable connections and the function of the second fusable connections to comply with Article 84 EPC.

These amendments are clearly supported by the original drawing illustrating an embodiment of the claimed invention and therefore meet the requirement of Article 123(2) EPC.

3. Whereas the subject-matter of combined Claims 1 and 2 is clearly novel with respect to any of the documents cited in the decision under appeal or in the European search report, the issue to be decided is whether it involves an inventive step.

3.1 D1 is concerned with the problem of providing spare columns of memory cells in a byte wide integrated memory.

In particular D1 shows on Figure 8 a byte wide memory wherein each byte includes n bits (n=2), each bit includes m sense amplifiers (m=1) and each sense amplifier has associated with it p columns of memory cells (p=16). Two spare columns of memory cells (redundant bit lines #1 and #2) are provided, as well as spare decoder means for switchably connecting a spare column to an associated spare sense amplifier (redundant data latches #1 and #2). The output of a spare sense amplifier can be connected to any data pad of the memory by means of an electrically conductive line and switching means (data pass devices) which are controlled by the state of fuses.

D1 indicates further that it is also possible not to use spare sense amplifiers, at the cost of having an increased bit line capacitance. In that case, according to D1, multiple bit switches would be needed for steering capability to any of the sense amplifiers (see page 296, left-hand column, last paragraph).

3.2 The skilled person is thus aware of the possibility of using sense amplifiers which are common both for the normal and the spare columns. It is then clear from D1 that such common sense amplifiers have to be placed in the data pad lines between the switching means (data pass devices) and the data pads. In that case the switching means would thus provide a connection between a conductive line associated with a spare column and each of the common sense amplifiers.

3.3 Therefore, the subject-matter specified in present Claims 1 and 2 differs from the prior art according to D1 only in that:

(a) a fusable connection is provided in each column of memory cells;

(b) a fusable connection is provided between the spare column and the conductive line;

(c) each switching means connected between the conductive line associated to a spare column and one of the sense amplifiers is controlled by a fuse connected between a potential source and the switching means.

3.4 As is apparent from D1, any column of the memory which is found defective should be isolated. To this effect D1 suggests in particular to inhibit the data latch associated with the defective column. As a possible alternative a defective column could be isolated by deselection of the associated bit switch (see page 296, right-hand column, lines 2-5). A further possible alternative which is immediately apparent to the skilled person is to electrically remove the defective column from the memory. As appears for example from D2 (see in particular page 857, right-hand column, paragraph B and Figures 8 and 9), an obvious possibility to achieve such removal is to use fusable connections. Thus feature (a) appears to be obvious to the skilled person.

3.5 The application in suit considers the possibility that even a redundant column could be found defective and for this reason has provided the first fusable connection in the spare column (feature (b)). Although D1 did not consider this eventuality the Board considers that the skilled person would be aware of it in view of D2. Indeed,

according to the cited passage of D2, if a spare column is itself found defective, it should also be electrically removed from the memory in the same way as any defective column and another spare activated. Therefore, feature (b) also appears to be obvious to the skilled person.

3.6 Regarding feature (c) the Board observes that D1 proposes to control the switching means (data pass devices) by means of DC voltages derived from the state of steering fuses (see page 296, right-hand column, sixth paragraph and page 297, left-hand column, lines 15-16). It is thus apparent from D1 that the switching means receive control voltages from a potential source through fuses which can be either conducting or non-conducting according to desired states of the switching means. Since each of the switching means has to be controlled individually, it appears logical to associate an individual fuse with each switching means. Thus, in view of D1, feature (c) appears to represent a possibility for controlling the switching means which is obvious to the skilled person.

3.7 The arguments submitted by the Appellant are not convincing.

In particular it is to be noted that, although D1 regards the provision of redundant sense amplifiers as preferable, it also clearly mentions the possibility not to use such redundant data latches. Thus the Board cannot agree that D1 would teach away from the invention.

It is accepted that D1 does not disclose that a particular fuse should be associated with each data pass device. However, as explained above, the skilled person would arrive at this feature in a logical and thus obvious manner by considering how the data pass devices are to be controlled. The advantage indicated by the Appellant would be achieved thereby without inventive ingenuity.

Finally, although starting from D1 different steps are necessary to arrive at the invention, it is noted that each of these steps relates to a separate problem to be solved. More precisely the steps corresponding to features (a) and (b) concern the problems of disconnecting a defective usual column and a defective spare column respectively, while the step corresponding to feature (c) relates to the problem of steering the switching means. In these circumstances each distinguishing feature can therefore be considered separately. Furthermore each distinguishing feature has been found obvious on the basis of suggestions already present in the prior art.

3.8 For these reasons the Board has come to the conclusion that the skilled person would arrive in an obvious manner at a memory having all the features specified in present Claims 1 and 2. Therefore, such a memory does not appear to involve an inventive step (Article 56 EPC).

Thus the request of the Appellant cannot be granted since a claim including the subject-matter of both Claims 1 and 2 could not be allowed (Article 52(1) EPC).

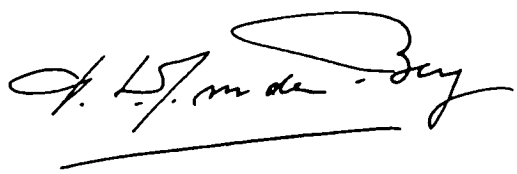
4. The other Claims 3-10 must share the fate of the combination of Claims 1 and 2. Furthermore they do not seem to include any feature which could involve an inventive step.

Order

For these reasons, it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:



M. Beer P.K.J. van den Berg