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Bezeichnung der Erfindung:
Title of invention:
Titre de l'invention : Semiconductor memory device having tunnel diodes

Klassifikation / Classification / Classement : G11C 11/34

ENTSCHEIDUNG / DECISION

vom / of / du 10 July 1990

Anmelder / Applicant / Demandeur : Kabushiki Kaisha Toshiba

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Art. 56

Schlagwort / Keyword / Mot clé : "Inventive step (auxiliary request: yes)"

Leitsatz / Headnote / Sommaire

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Case Number : T 600/89 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 10 July 1990

Appellant : Kabushiki Kaisha Toshiba
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Decision under appeal : Decision of Examining Division 067 of the European Patent Office dated 10 May 1989 refusing European patent application No. 83 102 232.2 pursuant to Article 97(1) EPC

Composition of the Board :

Chairman : P.K.J. van den Berg
Members : W.B. Oettinger
M. Lewenton

Summary of Facts and Submissions

I. European patent application No. 83 102 232.2, claiming a priority of 8 March 1982, filed on 7 March 1983 and published under No. 88 421, was refused by a decision of Examining Division 2.2.10.067 dated 10 May 1989.

The reason given for the refusal was that the memory cell defined in Claim 1, filed on 26 October 1987, lacked an inventive step having regard to the prior art.

In respect of the latter, reference was made to

D1: Electronics, Vol. 33, No. 22, (27 May 1960), pages 75 to 84,

D2: "Parametric and Tunnel Diodes" by K. Chung, Eaglewood Cliffs (NJ, USA) 1964, pages 169 to 171,

and to common knowledge in the field of flip-flop semiconductor memory cells.

In respect of dependent Claim 2, Claim 3 directed to a memory device, and dependent Claims 4 to 6, all filed on the same date, the Examining Division drew a similar conclusion, referring to statements in a preceding communication.

II. On 22 June 1989, the Applicant lodged an appeal against that decision requesting its cancellation, and paid the appropriate fee.

On 24 August 1989, the Appellant filed a statement of grounds contesting the Examining Division's view.

III. In a communication pursuant to Article 11(2) of the Rules of Procedure of the Boards of Appeal, the Board cited

D3: US-A-4 187 602

documenting the aforementioned common knowledge, and supported the Examining Division's view based on this prior art.

IV. In response to formal objections also made in that communication, the Appellant filed, on 8 June 1990, new Claims 1 to 3 and maintained that their subject-matter is inventive.

V. In oral proceedings held on 10 July 1990, the Appellant requested that

- the decision under appeal be set aside and a patent granted on the basis of
  - Claims 1 to 3 filed on 8 June 1990 (main request), or
  - Claims 1 and 2 filed in the oral proceedings on 10 July 1990 (first auxiliary request), or

- the procedure be continued in writing if the Board maintains its objection under Article 83 EPC (second auxiliary request).

Claim 1 (main request) reads as follows:

"A semiconductor memory device having at least one memory cell (MC11 to MCMN) including first and second tunnel diodes (TD1 and TD2) connected in series in a forward-bias direction between first and second power source terminals (VD and VS), the potential at a connection point between said tunnel diodes (TD1 and TD2) being set at one of a

level near a first trough (A1) potential of said second tunnel diode (TD2) and a level near a second trough (A2) potential of said first tunnel diode (TD1), thereby holding data in the memory cell,
characterised in that:

said memory cell (MC11 to MCMN) further includes a switching means (TR1) connected at one end to the connection point between said first and second tunnel diodes (TD1 and TD2) and at the other end to a bit line (BL01 to BL0M; BL11 to BL1M; B11 to BLM), said switching means (TR1) being ON/OFF controlled in accordance with a potential of a word line (WL1 to WLN), and a sense amplifier (SAC) for amplifying a potential read-out from said memory cell (MC11 to MCMN);

a potential of said bit line (BL01 to BL0M and BL11 to BL1M) is set at one of said first trough (A1) potential and said second trough (A2) potential during said switching means (TR1) is maintained to be on by making said word line (WL1 to WLN) active while first and second power source terminals (VD and VS) are held at substantially constant potentials, thereby setting the potential at the connection point between said first and second tunnel diodes (TD1 and TD2) at one of said first trough (A1) potential and said second trough (A2) potential so as to store data; and

said switching means (TR1) is turned on by making said word line active while first and second power source terminals (VD and VS) are held at substantially constant potentials, and the potential at the connection point between said first and second tunnel diodes (TD1 and TD2) is read-out to said bit line (BL01 to BL0M and BL11 to BL1M), so as to be amplified by means of said sense amplifier (SAC), thereby reading out the stored data."

Claim 2 of the main request is formulated as an independent claim but includes all the features of Claim 1, i.e. is, in substance, a dependent claim, as is Claim 3.

Claim 1 of the first auxiliary request reads as follows:

"A semiconductor memory device having at least one memory cell (MC11 to MCMN) including first and second tunnel diodes (TD1 and TD2) connected in series in a forward-bias direction between first and second power source terminals (VD and VS), the potential at a connection point between said tunnel diodes (TD1 and TD2) being set at one of a first current trough (A1) potential (VA1) of said first tunnel diode (TD1) and a second current trough (A2) potential (VA2) of said second tunnel diode (TD2), thereby holding data in the memory cell,
characterised in that:

said memory cell (MC11 to MCMN) further includes,
a switching means (TR1) connected at one end to the connection point between said first and second tunnel diodes (TD1 and TD2) and at the other end to a bit line (BL01 to BL0M and BL11 to BL1M), said switching means (TR1) being ON/OFF controlled in accordance with the potential of a word line (WL1 to WLN),
a reference potential generating means having at least a dummy cell (DC01 to DC0M and DC11 to DC1M) including third and fourth tunnel diodes connected in series in a forward-bias direction between said first and second power source terminals (VD and VS), for generating an intermediate potential (A3) at the connection between said third and fourth tunnel diodes set substantially in the middle between a first current trough (A1) potential of said third tunnel diode and a second current trough (A2) potential of said fourth tunnel diode, and

a sense amplifier (SAC) for comparing and amplifying a potential read-out from said memory cell (MC11 to MCMN) and the intermediate potential (A3) output from said dummy cell (DC01 to DC0M and DC11 to DC1M) of said reference potential generating means;

the potential of said bit line (BL01 to BL0M and BL11 to BL1M) is set at one of a level (VSS) near said first current trough (A1) potential of said first tunnel diode and a level (VDD) near said second current trough (A2) potential of said second tunnel diode while said switching means (TR1) is maintained to be ON by making said word line (WL1 to WLM) active and while said first and second power source terminals (VD and VS) are held at substantially constant potentials, thereby setting the potential at the connection point between said first and second tunnel diodes (TD1 and TD2) at one of said first current trough (A1) potential and said second current trough (A2) potential so as to store data; and

said switching means (TR1) is turned ON by making said word line active while said first and second power source terminals (VD and VS) are held at said substantially constant potentials, and the potential at the connection point between said first and second tunnel diodes (TD1 and TD2) is read-out to said bit line (BL01 to BL0M and BL11 to BL1M), so as to be compared with said intermediate potential (A3) generated by said reference potential generating means and to be amplified by means of said sense amplifier (SAC), thereby reading out the stored data."

Claim 2 (auxiliary request) corresponds to former Claim 3.

The other application documents on which the requested grant of a patent should be based are:

- the description and drawings as on file on 26 October 1987 (main request), or

- description page 1 filed on 26 October 1987,
  pages 1a, 2 and 5 filed in the oral proceedings (10 July 1990),
  pages 3 and 4 as published, and

  drawings sheet 1 to 3 as published (including Figs. 1 to 3) but Fig. 4 deleted (first auxiliary request).

VI. The Appellants' arguments submitted in support of these requests can be summarised as follows:

Main request

In the prior art (D1, D2), read-out of data stored in a series connection of tunnel diodes is performed by sensing a current when the supply voltage is shifted.

In contrast, the invention senses voltages and does that using a switch.

Even if it is true that this is known per se with other types of memory cells (D3), the fact that, although D1 and D2 are relatively old and there was clearly a need for improving the tunnel diode memory cells known from these documents, nobody applied, to these tunnel diode memory cells, the idea suggested by D3, may be taken as an indication that it was not obvious to do so.

First auxiliary request

Particularly the use of a tunnel diode dummy cell as a reference potential generating means is not suggested by any of the prior art documents on file.

The use of such dummy cells (DC in Fig. 1) has the advantage that they are cheaper to fabricate from tunnel diodes than the resistors which must otherwise be used as voltage dividers (Fig. 4).

As to the feasibility of this embodiment, reference should be made to the description, in particular to the paragraph bridging pages 4 and 5 and referring to Fig. 3, and to the second paragraph of page 5.

Reasons for the Decision

1. The appeal is admissible (Articles 106 to 108 and Rule 64 EPC).

2. The amendments made to the application documents are admissible (Article 123(2) EPC):

2.1 Claim 1 (main request) is based, in essence, on the original Claim 1, further specified in the following respects:

- the "predetermined" level at which the connection point between the tunnel diodes is set, is specified as being near a "trough" potential, this situation being derivable from Fig. 2;

- the switching means is specified as being controlled by a word line potential, this feature being described with reference to Fig. 1;

- the memory cell is specified as including a sense amplifier for amplifying a read-out potential, this feature being derivable from Figs. 1 and 3 and their description;

- the second paragraph of the characterising portion of Claim 1 only recites the function of the device when data is being stored, this function being disclosed on page 3, line 30 to page 4, line 21;

- the last paragraph of the characterising portion only recites the function of the device when data is being read-out, this function being disclosed in particular on page 5, lines 8 to 16.

2.2 Claim 1 (main request) being, however, unallowable for other reasons (cf. paragraph 4 below), no decision is required on the question whether (formally independent, in substance dependent) Claim 2 and (dependent) Claim 3 are admissible under Article 123(2) EPC or not.

For the same reason, it is not relevant that the statement of claims is inconsistent with the description (of the embodiment of Fig. 4 which has no sense amplifier), or vice versa.

2.3 Claim 1 of the first auxiliary request is based, in essence, on the original Claim 3, except for the express mention (in the original Claim 2) of the further "switching means", but further specified in the same respects as Claim 1 of the main request and, in addition thereto, in the following respects:

- the tunnel diodes of the dummy cell are similarly series connected as those of the memory cell (cf. Fig. 1) and the dummy cell constitutes a reference

(i.e. comparison) potential generating means (cf. page 5, second paragraph), and the reference potential generated lies substantially in the middle between the A1 and A2 potentials (cf. page 4, second paragraph);

- the sense amplifier compares (i.e. subtracts) the read-out and reference potentials (cf. page 5, second paragraph).

2.4 Insofar as the further "switching means" appears to be absent from Claim 1 (first auxiliary request), this claim seems to claim only a subcombination of the subject-matter of the original Claim 3 since that claim included, by its reference to Claim 2, said further "switching means".

However, in the present case this fact does not render Claim 1 inadmissible. It is clear from the last characterising feature of that claim that the reference potential must only be generated during those time periods in which a comparison is made with the read-out potential, and it is therefore clear that some switching of that reference potential to the reference bit line (BL11) should take place in a similar way as the tunnel diode memory cell node potential is switched (by TR1) to the bit line (BL01). It is therefore considered that the further "switching means" are still implicit in the claim.

2.5 Claim 2 (first auxiliary request) derives its admissibility from the original Claim 5.

2.6 The amendments made to the description and the drawings are confined to amendments necessary for meeting the requirements of Rule 27(1)(c) and (d) and Rule 34(1)(c) EPC.

3. As to patentability, novelty of the subject-matter claimed in either version is not at issue.

4. It is therefore left to be decided first, whether the subject-matter of Claim 1 (main request) involves an inventive step.

In the opinion of the Board, this is not the case for the following reasons and the Appellants' main request must therefore be rejected:

4.1 Semiconductor memory devices of the kind defined in the precharacterising portion of Claim 1 are known from D1, in particular Fig. 14, and D2, in particular Fig. 12-11(a).

According to this prior art, storing of data is accomplished by applying a signal to the junction between the tunnel diodes, cf. D1 page 83, left-hand column, line 1, and D2 page 171, first paragraph, and "input" in Fig. 12-11(a).

Read-out of data may, according to D1, page 83, left-hand column, lines 5 to 7, be accomplished by shifting the power source voltage and sensing the current variation polarity on the information line.

According to D2, page 171, second paragraph, it may be accomplished by sensing, if the power source voltage is perturbed, the voltage variation direction on the junction between the tunnel diodes, but from Fig. 12-11(d) it would seem to appear that what varies significantly with the power source voltage, is the current through the tunnel diodes (A-A', B-B').

4.2 In any case, however, in the opinion of the Board it would immediately follow from D1 that, particularly in a memory matrix, it would be an appropriate alternative to selection by address lines, to select the proper tunnel diode cell via a switch between its diode junction and the information line. This the more so as exactly this kind of selection is known from D3 (MOS switch 11) with similar storage cells using field implanted resistor pairs (12,13) instead of tunnel diode pairs.

Further it would, in the opinion of the Board, be immediately apparent to the person skilled in the art when viewing Fig. 12-11(d) of D2 that the stored data can be read out of a tunnel diode memory cell exhibiting the characteristics depicted in that Fig., by sensing whether the potential (or voltage with respect to a reference potential 0) at the diode junction has the value at A(-V2) or at B(V2) at the times where read-out shall take place, i.e. via a properly controlled switch. This, again, the more so as D3 suggests such a switch.

4.3 The Appellants' counter-arguments are, in the circumstances, unconvincing.

The mere fact that, in spite of the age of D1 and D2 of about two decades and that of D3 of several years, counted from the priority date of the present application, the search report has not brought to light any novelty destroying document, does not indicate that the claimed solution was unobvious. Said fact may have other reasons. No reason is seen why the person skilled in the art should have had, despite a longfelt need, a general prejudice, based on technological facts, against the solution claimed, which prejudice could have been regarded as an indication of non-obviousness.

5. In contrast, the subject-matter of Claim 1 of the first auxiliary request is regarded as involving an inventive step essentially for the following reasons:

5.1 None of the prior art documents on file suggests the particular kind in which the reference potential for read-out is generated, viz. by a dummy cell with tunnel diodes as claimed.

5.2 The obvious way of generating an intermediate potential between two given potentials which lie near the potentials of a power source would be using a potentiometric voltage divider, but such an embodiment (original Fig. 4) is not claimed any more.

5.3 Using, instead, two tunnel diodes connected in series is clearly not obvious because, prima facie, this idea is against the teaching of both D1 (page 82, left-hand column, third paragraph) and D2 (page 171, first paragraph) that the intermediate potential point, see in Fig. 12-11(d) of D2, in the I-U-characteristics of such a circuit is unstable.

It is accepted that it is the Appellants' discovery that the circuit can nevertheless be forced to take this point as its working point at least temporarily, viz. during read-out, i.e. via a switch.

It may be added that, apparently, this solution has certain advantages, for instance at its fabrication but possibly also in its behaviour in use, and is therefore useful.

6. Since no observation appears necessary in respect of the other documents filed for the first auxiliary request, this request is allowed and consideration of the Appellants' second auxiliary request unnecessary.

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.

2. The Appellants' main request is rejected.

3. The case is remitted to the first instance with the order to grant a patent on the basis of the first auxiliary request, i.e. with the following application documents:

   Description: page 1 filed on 26 October 1987,
   page 1a, 2 and 5 filed on 10 July 1990,
   pages 3 and 4 as published;

   Claims: 1 and 2 filed on 10 July 1990;

   Drawings: sheets 1 to 3 (Figs. 1 to 3) as published, with Fig. 4 deleted.

The Registrar: The Chairman:

M. Kiehl P.K.J. van den Berg