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Bezeichnung der Erfindung: Logic adder circuit

Title of invention:

Titre de l'invention :

Klassifikation / Classification / Classement : G06F 7/50

**ENTSCHEIDUNG / DECISION**

vom / of / du 25 April 1990

Anmelder / Applicant / Demandeur : N.V. Philips' Gloeilampenfabrieken

Patentinhaber / Proprietor of the patent /  
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Article 56

Schlagwort / Keyword / Mot clé : "Inventive step - yes"

**Leitsatz / Headnote / Sommaire**



Case Number : T 624/89 - 3.5.1

**D E C I S I O N**  
of the Technical Board of Appeal 3.5.1  
of 25 April 1990

**Appellant :** N.V. Philips' Gloeilampenfabrieken  
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**Decision under appeal :** Decision of Examining Division 065  
of the European Patent Office  
dated 25 May 1989 refusing European  
patent application No. 85 200 134.6  
pursuant to Article 97(1) EPC

**Composition of the Board :**

**Chairman :** P.K.J. van den Berg  
**Members :** W.J.L. Wheeler  
M. Lewenton

## Summary of Facts and Submissions

- I. Appellant's European patent application No. 85 200 134.6, filed on 7 February 1985, claiming priority from a previous application in the Netherlands dated 9 February 1984, was refused by a decision of the Examining Division dated 25 May 1989. That decision was taken on the basis of Claims 1 to 6 as originally filed.
- II. The reason given for the refusal was that the subject-matter of the claims did not involve an inventive step, having regard to common general knowledge and the following prior art document:  
  
D1: US-A-3 970 833.
- III. On 21 July 1989 the Appellant filed a notice of appeal against that decision. The appeal fee was paid on the same day. The statement of grounds was filed on 27 July 1989.
- IV. In response to a communication of the Board pursuant to Article 110(2) EPC, the Appellant filed on 27 March 1990 replacement pages 1 to 5 of description, replacement Claims 1 to 6 and details of the prior art circuits SN7483 and MC14008 acknowledged on page 1 of the description. In an accompanying letter dated 21 March 1990 it was stated: "We agree with the suggested amendments." That letter also referred to new drawings, but none appear to have been received.

V. The Appellant requests, in effect, that the decision under appeal be set aside and a patent granted on the basis of the following documents:

- Claims 1 to 6, filed on 27 March 1990;
- Description: pages 1 to 5, filed on 27 March 1990;
- Drawings, sheets 1/2 and 2/2 as originally filed on 7 February 1985, with the amendments to Figures 1 and 3 shown on the copies enclosed with the Board's communication pursuant to Article 110(2) EPC.

VI. Claim 1 is now worded as follows:

"1. A logic full-adder circuit for adding two binary numbers  $a$  and  $b$  which each consist of  $n$  bits,  $n$  being a natural number larger than or equal to 2, comprising an inverting OR-gate (1) and an inverting AND-gate (3) for each bit  $a_i$ ,  $b_i$  of the numbers  $a$  and  $b$ , where  $0 \leq i \leq n-1$ , said gates receiving the bit signals  $a_i$  and  $b_i$  in order to form an inverter OR-signal  $\overline{a_i+b_i}$  and an inverted AND-signal  $\overline{a_i \cdot b_i}$ , and also comprising a summing circuit (20) for forming a sum signal  $s_i$  of the bit signals  $a_i$  and  $b_i$  and an associated carry signal  $c_i$  and/or the inverse  $\overline{c_i}$  thereof, said full-adder circuit also comprising a carry look-ahead signal circuit (50) for generating a carry look-ahead signal  $c_n$  having the significance  $n$  from all inverted OR-signals and AND-signals  $\overline{a_i+b_i}$  and  $\overline{a_i \cdot b_i}$ , where  $0 \leq i \leq n-1$ , characterized in that each summing circuit (20) comprises a logic gate (5) which receives the bit signals  $a_i$  and  $b_i$  and the inverted AND-signal  $\overline{a_i \cdot b_i}$  in order to form a logic signal  $\overline{a_i \cdot b_i} \cdot (a_i+b_i)$  on a first output (11) thereof and the inverted logic signal  $\overline{a_i \cdot b_i} \cdot (a_i+b_i)$  on a second output (13) thereof, and also comprises electronic switches (7,9) which connect, under the control of the carry signal  $c_i$  and/or the inverse  $\overline{c_i}$

thereof, either the first output or the second output of the logic gate (5) to a first junction (15) in order to generate an inverted sum signal  $s_i$  on the first junction."

#### Reasons for the decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is, therefore, admissible.
2. As appears from paragraph 6 of the decision under appeal, the Examining Division's reason for refusing the present application is based on the assertion that the logic full adder circuit defined in Claim 1 differed from the logic full adder circuit in Figure 2 of D1 in that in Claim 1 the summing circuit "comprises electronic switches which connect, under the control of the carry signal  $c_i$  and/or the inverse  $\bar{c}_i$  thereof, either the first output or the second output of the logic gate to a first junction in order to generate an inverted sum signal  $\bar{s}_i$  on the first junction", while in Figure 2 of D1 the switches connect, under the control of the first output and/or the second output of the logic gate, either  $c_i$  or  $\bar{c}_i$  to a first junction to generate  $\bar{s}_i$ .
3. The Board notes that the Examining Division has not (either in the decision under appeal or in the correspondence preceding that decision) demonstrated which features of the circuit shown in Figure 2 of D1 are supposed to correspond to which features specified in Claim 1 of the present application.
4. The Board agrees with the Appellant that the circuit claimed in Claim 1 of the present application differs from the circuit shown in Figure 2 of D1 in more ways than the Examining Division asserted. In view of the wording "and

also comprising a summing circuit" in Claim 1, it is clear that the summing circuit (20) must be additional to the inverting OR-gate (1) and inverting AND-gate (3) mentioned earlier in the claim. Thus, the corresponding summing circuit in the circuit shown in Figure 2 of D1 could comprise items 52 to 54 and 58 to 62, but not the NAND and NOR gates 50, 51, since they correspond to the inverting OR-gate (1) and inverting AND-gate (3) mentioned in Claim 1. In the circuit shown in Figure 2 of D1, the bit signals  $a_i$  and  $b_i$  are fed only to the gates 50, 51. Consequently, as pointed out by the Appellant, the summing circuit shown in Figure 2 of D1 does not comprise a logic gate which receives the bit signals  $a_i$  and  $b_i$ , as specified in the characterising part of Claim 1.

5. In the opinion of the Board, D1 is no closer to the present invention than is the prior art acknowledged on page 1 of the present application.
6. As pointed out by the Appellant, the full adder circuit claimed in Claim 1 of the present application needs fewer gates than the prior art circuits and has only four gate delays (gates 3, 30, 40, 17) from the input of the bit signals  $a_i$  and  $b_i$  to the output of the sum signal  $s_i$  and only two gate delays (gate 1 or 3 plus gate 27) from the input of the bit signals  $a_i$  and  $b_i$  to the output of the carry signal  $c_{i+1}$ .
7. Starting from the prior art according to D1, or from either of the circuits SN7483, MC14008, the problem solved may be seen as to provide a faster full-adder circuit in which the number of components needed is reduced.
8. While the above stated problem may properly be regarded as one which a person skilled in the art could be expected to try to solve, in the opinion of the Board, in the absence

of any suggestion in the cited prior art, it would not be obvious to make all the changes necessary to adapt the prior art circuits in the manner specified in the characterising part of Claim 1 of the present application.

9. In the result, the Board takes the view that the circuit claimed in Claim 1 of the present application involves an inventive step over the cited prior art and the decision under appeal must therefore be set aside.
10. The amendments made to the claims, description and drawings are only for the purposes of adding reference signs in accordance with Rule 29(7) EPC, correcting obvious clerical errors and removing inconsistencies. In the opinion of the Board, the current version of the application complies with Article 123(2) EPC and meets the requirements for the grant of a European patent.
11. The Board has noticed several clerical errors in the documents filed on 27 March 1990, which are clearly inconsistent with the Appellant's intention, expressed in the letter dated 21 March 1990, to agree with the amendments suggested by the Board. These errors are:

page 2, the last word in line 2 should read "signals",  
 page 4, line 12, "inverter" should read "inverted",  
 page 4, line 23, " $\overline{a_i \cdot b_i} \cdot (a_i \cdot b_i)$ " should read  
 $\overline{a_i \cdot b_i} \cdot (a_i + b_i)$ ,  
 page 4, line 24, " $\overline{a_i \cdot b_i} \cdot (a_i \cdot b_i)$ " should read  
 $\overline{a_i \cdot b_i} \cdot (a_i + b_i)$ ,  
 Claim 6, page 8, line 1, "inverted" should read  
 "inverter",  
 Claim 6, page 8, line 2, "gate" should be inserted  
 before "electrodes".

**Order**

**For these reasons, it is decided that:**

1. The decision under appeal is set aside.
2. The case is remitted to the first instance with the order to grant a patent on the basis of the Appellant's request (paragraph V above), with correction of the clerical errors listed in paragraph 11 above.

**The Registrar:**

**The Chairman:**

**M. Beer**

**P.K.J. van den Berg**