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Bezeichnung der Erfindung:
Title of invention:
Titre de l'invention : Semiconductor memory device with a refresh mechanism

Klassifikation / Classification / Classement : G11C 11/24

ENTSCHEIDUNG / DECISION

vom / of / du 14 December 1990

Anmelder / Applicant / Demandeur : Kabushiki Kaisha Toshiba

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Art. 56

Schlagwort / Keyword / Mot-clé : "Inventive step after amendment of the claim (yes)"

Leitsatz / Headnote / Sommaire

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Case Number : T 736/89

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 14 December 1990

Appellant : Kabushiki Kaisha Toshiba
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Decision under appeal : Decision of Examining Division 067 of the European Patent Office dated 10 May 1989 refusing European patent application No. 83 307 761.3 pursuant to Article 97(1) EPC

Composition of the Board :

Chairman : P.K.J. van den Berg
Members : W.P.H. Riewald
F. Benussi

Summary of Facts and Submissions

I. European patent application No. 83 307 761.3, claiming priority of an application in Japan of 27 December 1982, filed on 20 December 1983 and published on 29 August 1984 was refused by a decision of the Examining Division 067 dated 10 May 1989 which was based on Claims 1 to 8 filed with letter of 19 September 1988.

II. The reason given for the refusal was that the subject-matter of Claim 1 lacked inventive step and that also the dependent claims and the other documents of the application did not contain any patentable subject-matter.

III. The Examining Division based its decision on the documents

D1: US-A-3 737 879, and
D2: US-A-4 292 676.

A further document

"Triebel, Handbook of Semiconductor and Bubble Memories" Prentice-Hall, Inc., Englewood Cliffs, N.J. 1982

had only been cited in a first communication of the Examining Division in respect of a dependent claim.

IV. On 7 July 1989 the Applicant lodged an appeal against the decision by telex which was confirmed by a letter received on 10 July 1989. The appeal fee was paid on 7 July 1989. A Statement of Grounds of Appeal was received on 19 September 1989.

The Appellant held that the treatment of the case by the Examining Division was not reasonable and put particular emphasis on the use of "a specific refresh timer" in the

invention as a distinction over the prior art disclosed in the citation D1.

V. In a communication dated 15 February 1990 and accompanying summons for oral proceedings, the Rapporteur made additional reference to the document

D3: US-A-3 533 089

(cited in D1 as prior art) and made an analysis of the features claimed in Claim 1 in view of document D1. He came to the conclusion that "a specific refresh timer" was not part of the specification of Claim 1. In addition, he drew attention to a feature derivable from the description in connection with the function of the address counter in Claim 1: a delay circuit stopping the incrementation of the address counter until refreshing of a word line is completed. It was indicated that a clarification of these details in Claim 1 might be regarded as a minimum requirement in order to arrive at a claim meeting the requirements of clarity and support by the description (Article 84 EPC), but that, in view of the combined teachings of the documents D1 and D2, the question of inventive step would still have to be discussed.

VI. Oral proceedings were held on 23 May 1990 at which the Appellant filed a hand-written new Claim 1 and the Appellant was given the opportunity to file amendments in accordance with the instructions given by the Board.

VII. With letter of 20 July 1990, the Appellant filed a new Claim 1 and adapted pages of the description, which documents were still further amended with letter of 9 November 1990 in reply to objections by the Board in respect of an acknowledgement of the pertinent prior art.

With these amendments the Appellant requests that the decision under appeal be set aside and that a patent be granted on the basis of the following documents:

Description: pages 1 and 4 to 12 as published;
pages 2, 2a and 3, received on 12 November 1990 with letter of 9 November 1990;

Claim 1: received on 12 November 1990 with letter of 9 November 1990;

Claims 2-8: received on 22 September 1988 with letter of 19 September 1988;

Drawings: sheets 1/6 to 6/6 as published.

VIII. The independent Claim 1 reads as follows:

"A semiconductor memory device comprising a plurality of memory cells (100) each consisting of one transistor (1) and one capacitor (2) a plurality of word lines (W_L) for addressing said memory cells, a plurality of digit lines (Wd) for reading and/or writing the data of said memory cells, an access control means (101,103) for accessing said memory cells by selecting said word lines, a refresh clock Rc for starting the refresh period at fixed intervals, a refresh control means (107) for successively selecting said word line connected to each of said memory cells and refreshing said memory cells word line by word line in the refresh period; characterised by

a pulse generator (11) generating pulses at intervals shorter than the time taken to refresh one word line, and a timing means (102) connected to each of the word lines, each of said timing means (102) being so arranged that it is activated whenever the word line connected to it is selected during an access period and being arranged to

supply a "refresh not required" signal until a predetermined time has elapsed, said refresh control means (107) being arranged to detect said "refresh not required" signal and to then select the next word line, and wherein said refresh control means (107) includes;

a row address counter (10) for successively selecting said word lines in accordance with pulse signals from said pulse generator, a first circuit means (12) for detecting the data in said row address counter and emitting a pulse signal indicating the end of said refresh period, and a second circuit means (15) which is so arranged that

(a) when said "refresh not required" signal is supplied from said timing means, the row address counter is incremented by 1 without a refresh signal being issued to the corresponding word line; and

(b) when said "refresh not required" signal is not supplied, the incrementation of the row address counter is delayed, a refresh signal is issued, and the row address counter is incremented after completion of the refresh process for the corresponding word line."

IX. The Appellant's submissions in support of the patentability of the subject-matter of Claim 1 can be summarised as follows:

The invention starts from a prior art as explained on page 2 of the description, lines 2 to 9, according to which refresh periods are started at fixed intervals of, e.g. 2 msec, and all the word lines of the semiconductor memory device are successively refreshed within each refresh period.

With the characterising features two problems of this prior art are solved:

- When a refresh is not required for a particular word line, because this word line was accessed during the access period preceding the refresh period, a refresh signal is not issued to this particular word line. Thereby the consumption of electric power during the refresh period is reduced.

- The refresh control means selects the word lines during each refresh period at intervals shorter than the time taken to refresh one word line if a refresh is not required. Only if a refresh is required for any particular word line the incrementation to the next word line is delayed so that the refresh process can be completed. Thereby the refresh period is shortened.

According to D1 refresh periods are not started at fixed intervals but always when a word line has not been accessed for a predetermined interval. Thus, the starting time of any refresh period is unpredictable. Furthermore, no means are derivable for cutting down the time of a refresh period of the encoder and scan circuit 72.

It is admitted that D2 discloses a system in which an accessed word line can be skipped during a refresh period. However, in this arrangement, an entire block of "auxiliary" memory is required to memorise the addresses of the already refreshed locations, resulting in a considerably more complex and expensive circuit configuration than the claimed invention.

It is not conceivable how the teaching of D2 - which clearly requires a regular cyclic operation - could, without hindsight, be realistically combined with the inherently intermittent operation of the circuitry of D1.

Reasons for the Decision

1. The appeal is admissible.

2. **Admissibility of the amendments**

Claim 1 is a combination of the original Claims 1 and 2 with incorporation of the following additional features:

- The refresh period is started at fixed intervals by a refresh clock Rc. This corresponds to the disclosure in the description, page 5, lines 7 to 9 and page 6, line 21 onwards.

- The pulse generator (11) generates pulses at intervals shorter than the time taken to refresh one word line. This is disclosed on page 7 of the description, lines 9 to 18.

- A refresh signal is not issued when a "refresh not required" signal is supplied, i.e. refreshing a word line previously assessed is skipped quickly; cf. description page 7, lines 9 to 14.

- If a refresh is required, the incrementation of the row address counter is delayed, a refresh signal is issued and the row address counter is incremented after completion of the refresh process for the corresponding word line. This corresponds to the disclosure in the description, page 6, lines 4 to 7.

It follows that all the amendments in Claim 1 meet the requirement of disclosure in the originally filed application documents (Article 123(2) EPC).

The same applies to the newly filed pages 2, 2a and 3 of the description, which acknowledge the pertinent prior art (US-A-3 737 879 and US-A-4 292 676) and which are adapted to the wording of Claim 1, and to the Claims 2 to 8, which correspond to the original Claims 3 to 9.

3. **Novelty**

All three documents D1 to D3 deal with semiconductor memory devices comprising a plurality of memory cells, a plurality of word lines for addressing said memory cells, a plurality of digit lines for reading and/or writing the data of said memory cells and access control means for accessing said memory cells by selecting said word lines. A detailed representation of the memory cells each consisting of one transistor and one capacitor can be found in D3 (e.g. Fig. 6) which is referred to in document D1.

Due to leakage of the charge of the capacitor of the memory cell such dynamic semiconductor memories require means for refreshing the memory cells within certain time intervals. The timing of the refresh actions is in D3 only touched upon (column 1, lines 24 to 27 and column 4, lines 36 to 41).

3.1 The present application starts from a prior art with refresh periods starting at fixed intervals (e.g. 2 msec.) by a refresh clock and the word lines being in uninterrupted succession refreshed in each refresh period. Each word line is thereby refreshed irrespective of its possibly having been accessed (and thus refreshed) during the foregoing access period (description, page 2, lines 2 to 19).

Starting from this prior art the invention seeks to solve two problems (description, page 2, lines 20 to 26):

- reduction of consumption of electric power during the refresh period, and

- shortening of the refresh period itself.

These problems are solved in accordance with the characterising portion of Claim 1 whose most essential features are:

- Timing means (102) connected to each of the word lines for applying a "refresh not required" signal for a predetermined time interval after any selection of the respective word line during an access period.

- A pulse generator (11) generating pulses for the incrementation of a row address counter (10) at intervals shorter than the time taken to refresh one word line.

- Second circuit means (15) responsive to the "refresh not required" signal with the effect that the incrementation of the row address counter is delayed if refresh of a particular row is required.

3.2 A semiconductor memory device which has a number of features in common with the claimed semiconductor device is disclosed in D1:

This memory device comprises a plurality of memory cells in a memory matrix 14, each memory cell consisting of one transistor and one capacitor (document D3 cited in D1, column 3, line 12). The memory cells are addressed by a plurality of word lines (D1: row conductors 24A to 24H). The data of the memory cells are read or written by a plurality of digit lines (column conductors 26). A row select array 16 controls the access to the memory cells by

selecting the word lines 24A to 24H. A refresh control means (self refreshing system 12) successively selects the word line connected to each of the memory cells and refreshes the memory cells word line by word line in a refresh period (encoder and scan circuit 72; cf. in particular column 6, lines 51 to 56).

In contrast to the precharacterising part of the present Claim 1, the refresh periods according to D1 are not started at fixed intervals but only when one or more word lines need refreshing (column 4, lines 15 to 21 ("mandatory" refresh)). The refresh periods are started through an OR gate (44) if one of a number of timing means (counters 42A to 42H) indicates that a respective row of the memory matrix (the signals on conductors 46A to 46H are, by means of the decoder 40, in perfect synchronism with the outputs of the row select array 16, Fig. 1) requires refresh (D1, column 4, lines 16 to 56 and column 5, lines 11 to 27).

The statement that the timing means supplies a "refresh required" signal after a predetermined time has elapsed can be regarded as equivalent to a statement that a "refresh not required" signal is supplied until the predetermined time has elapsed. Insofar, the application of the timing means is known per se.

In further agreement with the subject-matter of the present Claim 1 in D1 a pulse generator generates pulses in order to increment a row address counter (encoder and scan circuit 72) during the refresh period and to effect a refresh operation on a particular word line only if a "refresh required" signal is outputted from the respective timing means (column 6, line 35 to column 7, line 15). In contrast to the presently claimed subject-matter, however, in D1 no means are provided by which the time intervals

between the pulses incrementing the encoder and scan circuit are adapted to the presence or absence of a signal requiring refresh.

A further embodiment of D1, depicted in Figure 3 avoids this uniform scan of the word lines irrespective of their requirement of refresh but follows a different concept than the present application. Whereas the present application maintains the use of a row address counter and only delays its incrementation if refresh is required for a particular word line, Figure 3 of D1 provides circuitry (scan circuit 70) logically combining the output signals of the timing means (counters 42) that have reached their final stage in a way that allows the scanning of only the respective word lines for refreshment. "Refresh cycle complete pulses" control the shifting from one word line to the next word line to be refreshed (column 8, line 13 onwards, in particular lines 13 to 30 and column 9, lines 48 to 57).

3.3 Document D2 discloses a semiconductor memory device in which a refresh oscillator 100 controls a refresh counter 106 with a period equal to 1/2 the interval T at which the memory device 112 would have to be refreshed divided by the number of memory rows (column 4, lines 29 to 34). Also this document deals with the problem to reduce the number of refresh actions by skipping the refresh action for those word lines which have recently been accessed (column 2, lines 10 to 21 and 39 to 42).

However, the information whether the particular row being addressed by the refresh counter 106 should be refreshed during a current refresh cycle or alternatively, could be skipped is not derived from timing means as in the present application. Instead of this, information of access to each of the word lines of the memory device is stored in a particular storage location of an auxiliary memory. This

stored information is then utilised by the refresh counter and refresh oscillator to determine whether the particular row being addressed should be refreshed or not (see in particular column 6, lines 3 to 15).

The Board notes that D2 does not teach to alter the period at which the refresh counter 106 is incremented. Thus, the period of a complete refresh cycle, covering all the word lines of the memory device, is not shortened.

3.4 The subject-matter of Claim 1 is therefore deemed to be novel.

4. **Inventive step**

It follows from the above analysis of the prior art that it is already known to skip refresh actions in dynamic semiconductor memory devices for recently accessed word lines. Thereby two main concepts can be distinguished:

- D1 teaches to determine for each word line separately the time elapsed since the last read or write or refresh action has taken place and to trigger a refresh action only if the maximum allowable time has elapsed.

- D2 addresses, by means of a refresh counter, all the word lines at fixed intervals. The period of the refresh counter is so determined that the refresh action can be skipped for each particular word line which has been accessed after its foregoing refresh action, so that the next refresh action for that word line comes sufficiently in time to avoid loss of memory information.

The addresses of the accessed word lines are stored in an auxiliary memory in order to control the skipping action.

Thus, the use of the timing means in the prior art (D1) is conceived to refresh each word line as late as possible and, therefore, at irregular intervals determined by the unpredictable normal access actions. The use of an auxiliary memory (D2), on the other hand, is typical for the presence of a refresh counter scanning the addresses at regular intervals determined by a specific refresh timer.

The Appellant's argument that the combination of details from the two teachings, i.e. the combination of the use of timing means known from D1 and the use of a specific refresh timer known from D2, was not so obvious for a skilled person, appears therefore to be justified.

Moreover the row address counter of the present invention normally increments at intervals shorter than the time taken to refresh one word line and a delay necessary for the correct execution of a refresh action is only introduced when there is no "refresh not required" signal. This novel concept of using a row address counter with two different rates of incrementation is not derivable from the documents cited in the proceedings. Nor can it be regarded as a matter of any general background knowledge.

The Board is therefore satisfied that the subject-matter of Claim 1 involves an inventive step within the meaning of Article 56 EPC.

5. The independent Claim 1 is therefore allowable, and the same applies to the dependent Claims 2 to 8 since they specify embodiments of the subject-matter of Claim 1 and comply with the provisions of Article 84 and Rule 29 EPC.

6. Attention should be paid to an amendment of some clerical imperfections:

- Claim 1, line 3: a comma is to be set after "capacitor (2)", and
  line 8: substitute "a" for "the".

  The same amendments are to be made on page 2, last paragraph.

- page 1, last line to be deleted.

- page 4, line 10: substitute "numeral" for "numerals".

- page 5, line 4, fourth word: substitute "controls" for "control".

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a European patent with the documents specified in section VII and the amendments set out in section 6.

The Registrar: The Chairman:

P. Martorana P.K.J. van den Berg