BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS | BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE | CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

Publication in the Official Journal ~~Yes~~ / No

File Number: T 247/90 - 3.5.1

Application No.: 84 402 451.3

Publication No.: 0 144 268

Title of invention: Method for controlling buffer memory in a data processing apparatus

Classification:

D E C I S I O N
of 28 April 1992

Applicant: FUJITSU LIMITED

Headword:

EPC Article 56

Keyword: "Inventive step (yes)"

Headnote

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number : T 247/90 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 28 April 1992

Appellant :

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Decision under appeal :

Decision of Examining Division of the European Patent Office dated 6 October 1989 refusing European patent application No. 84 402 451.3 pursuant to Article 97(1) EPC.

Composition of the Board :

Chairman : P.K.J. Van den Berg
Members : R. Randes
W.M. Schar

Summary of Facts and Submissions

I. European patent application No. 84 402 451.3, filed on 30 November 1984 and published on 12 June 1985 (publication No. 0 144 268), claiming priority from two previous applications in Japan, was refused by a decision of the Examining Division dated 6 October 1989.

II. The decision was based on Claim 1 received on 12 May 1989.

The reason given for the refusal was that the subject-matter of Claim 1 lacked the required inventive step in the light of the following two documents:

D1: IBM Technical Disclosure Bulletin, Volume 25, No. 11B, April 1983, pages 5962-5966, New-York, US, Driscoll et et al.: "Design for improved Cache Performance via Overlapping of Cache Miss Sequences".

D2: EP-A-0 054 888.

In the decision it was said that the Latent-hits-circuit of D1 always permitted access to any word of a block undergoing transfer under the condition that the words had already been stored into the buffer memory. The circuit of D1 thus appeared to work whether the access was to the first word of the block or not. Thus, an access (read or write) could be granted as soon as the word was in the buffer.

When starting from the teaching of D1, the problem to be solved, therefore, appeared to be, to have in case of a block transfer, the requested word available for reading by the processor as soon as possible and therefore to permit

an immediately succeeding write operation to the same address even if the block transfer was not yet finished.

D1 was said to be silent about which word was first transferred from the main memory, but D2 disclosed that a block transfer was started with the word requested, whereby the arrangement permitted accesses to a buffer by a CPU during a block transfer from a main- to a buffer memory. Moreover said arrangement included a buffer by-pass from a buffer input register 40, 41 to a buffer output register 44, 45 (Figure 4) and, therefore, permitted immediate transfer of the first word to the CPU.

When thus using the teaching of D2 in order to adapt the method according to D1, also a subsequent "write to the same address as the requested word" would be obvious to the skilled man.

III. A Notice of Appeal was filed against this decision on 14 December 1989 and a Statement of Grounds of Appeal was submitted on 18 January 1990.

The Appellant pointed out that D1 did not suggest by-passing the beginning word of data to a calculation portion and the system of D2 was simply concerned with an access to a buffer storage from a basic processing unit even during a block transfer.

Moreover, the Appellant argued that the decision of refusal apparently was relying on the misunderstanding that the method of the application was erroneously interpreted as utilizing "a flag for indicating a word for which the registration to a buffer is completed", although in the method according to the only claim no such utilisation was carried out. The Appellant did not consider parts of the application which suggested such a "flag" (the BMC block in

original Figures 4B and 9 and the corresponding original text) as part of the invention.

Another misunderstanding in the decision appeared to be that the "fetch and store" instruction was confused with the execution of a casual succession of a fetch instruction and a store instruction. In the case of the "fetch and store" instruction, it was possible to automatically proceed only if the instruction was acknowledged as a "fetch and store". Thereby a "flag" as shown in Figure 9 of the application was not used, since the time relationship between the fetch and the store was predetermined, i.e. the addresses and the word positions in blocks were the same.

IV. After communications, wherein the clarity of Claim 1 was discussed, the Appellant on 6 March 1992 filed the following sole claim:

"A method for controlling a buffer memory (BM) that stores a copy of a portion of a main memory (MM), said buffer memory and said main memory forming part of a data processing apparatus with a central processing unit, said method being operative during a fetch-and-store instruction to carry out reading of data from an address, for calculation, and subsequent writing of results of the calculation into the same address, and comprising the steps of:

detecting whether the address in question exists in said buffer memory (BM), where:

in the case where the result of said detection is affirmative, the data from the address in question is read out from said buffer memory (BM) and results of the calculation are subsequently written into the address in question; and

in the case where the result of said detection is negative, there are performed the steps of:

issuing a request for the main memory (MM) to output data from a block which contains the address in question in the main memory,

transferring the read data in the block from the main memory (MM) to a block of the buffer memory (BM), such that the data corresponding to the address in question is placed at the beginning of said read data block,

said method being characterized in that it then further comprises the steps of:

by-passing said data corresponding to the address in question to a calculation portion,

writing said transferred data into the buffer memory starting with the data corresponding to the address in question, and

writing a result of the calculation into the location of the buffer memory corresponding to the address in question in the cycle next to the cycle of the writing of said data corresponding to the address in question, and, after writing of the result of the said calculation,

transferring the remaining data from said block in the main memory to the remaining locations in the block in the buffer memory."

The Appellant requests that the decision under appeal be set aside and a patent granted on the basis of the said sole claim and the following documents:

Description:

Pages 7, 9 and 10 as originally filed,
Page 5 as filed on 12 May 1989,
Page 6 as filed on 22 March 1991,
Pages 1 to 4, 8 and 11 as filed on 6 March 1992.

Drawings:

Sheets 1/10 to 8/10 as originally filed.

Reasons for the Decision

1. The appeal is admissible.

2. The sole claim has been delimited against prior art as acknowledged by the Appellant in the introductory part of the description. Moreover some amendments have been made in order to clearly identify the claimed method. Thus, the valid claim clearly identifies the said instruction as a "fetch-and store" instruction, states that the data from the block in the main memory are transferred to a block in the buffer memory and makes clear that after the writing of the said result of the calculation, the remaining data from said block of the main memory are transferred to the remaining locations in the block of the buffer memory. Also the last paragraph of original Claim 1 has been deleted, as it was redundant and did not contribute to the clarity. The sole claim meets the requirements of Article 123(2) EPC.

3. The issue to be dealt with is whether the subject-matter of the sole claim involves an inventive step.

3.1 The Board is of the opinion that the closest prior art is the one disclosed in the original description (page 5, line 11 to page 6, line 2 and page 11 concerning Figure 8), which prior art has been acknowledged by the delimitation of the sole claim.

3.2 The Examining Division in its decision, however, considered the teaching of D1 as the closest prior art.

In the Board's view, D1 discloses a system having a "Latent Hit Map", which always permits access to any word of a block undergoing transfer under the condition that the words have already been stored into the buffer memory as indicated by the "Latent Hit Map". It is, therefore, correct, as the Examining Division states (page 3 of the said decision, penultimate paragraph), that the circuitry of D1 works whether the access is to the first word of the block or not and that an access (read or write) may be granted as soon as the word is in the buffer. Thus, this document discloses a general method to achieve access to a word already in the buffer when using a "Hit Map".

There is no hint in the document that the transferred data should be written into the buffer memory with the word of the requested address placed as the beginning word of the data. Moreover, the teaching of D1 does not give any hint to by-pass the beginning word of data to a calculation portion in connection with the transfer operation from the main memory. However, just this operation makes it possible to execute the writing-step of a calculation immediately after the transfer operation from the main memory.

Therefore, it seems that the problem defined by the Examining Division (see under II above) cannot be deduced from the circuitry disclosed in D1 (having a "Latent Hit Map") and applied to a system lacking a validity flag

register. On the contrary, it appears that said problem is not objectively derived from the prior art and inadmissibly appears to incorporate parts of the solution offered by the invention (cf. T 229/85, O.J. EPO 1987, page 237, especially page 240, third paragraph and T 99/85, O.J. EPO 1987, page 413).

3.3 It is correct that according to D2 a block transfer is started with the word requested and that a buffer by-pass from a buffer input register (40,41, Figure 4) to a buffer output register (44,45) permits immediate transfer of the first word to the CPU (see page 4, first paragraph in the said decision). It is nowhere stated in the said document that a calculation is performed in the CPU or indicated that a result from such a calculation can be written into the address of the said requested beginning word.

According to the embodiment disclosed in D2 the block is transferred in four separate periods, each time as two doublewords (compare Figure 3 and pages 15 to 17). However, the first word to be transferred is delayed in a register during one cycle (when the second word is transferred to another register) and, therefore, arrives at the buffer storage together with the second word.

The aim of the system according to D2 is to increase the processing speed per instruction (see pages 8 and 9). Nowhere is it stated that processed data could be returned to a buffer memory address of a special requested word. The general idea disclosed in this document appears to be the creation of periods (during the transfer of a block) which are made available for an access to the buffer memory. This opinion appears to be underlined by the statement at the end of the description, that 8n-byte data can be transferred in n cycles and may be written into the buffer storage in one access cycle. Thus apparently many words can

be written simultaneously. However, the more words are written simultaneously, the larger the delay will be between the transfer of the first word to a register and the final transfer to the buffer storage.

Therefore, the teaching of D2 appears to teach away from the solution according to the present application and a skilled man, when reading D2, would not consider in which way a result of a calculation can quickly be written into the buffer address corresponding to the first word transferred. Thus, he would neither use the document for deriving a problem as suggested by the Examining Division, nor would he use the document in combination with D1 and so arrive at the invention.

3.4 The prior art as now acknowledged by the Appellant (see under paragraph 2 above) does not give any indications either to the skilled person how to arrive at the solution according to the sole claim. Although the solution in an ex post facto analysis can appear to be simple, it is the opinion of the Board that the subject-matter of the sole claim is not obvious to a skilled man (Article 56 EPC).

It appears that the general problem formulated by the Appellant (in the present description, page 1, lines 11 to 15 - "... writing of operand data into a block of the buffer memory is speeded up to realize high speed operation of a central processing unit...") is correctly derived from the prior art disclosed in the procedure. In fact, it appears that also the teachings of D1 and D2 are concerned with problems that could fall within the said general problem. However, the solution according to the present application is as shown above completely different from the ones of the said documents and cannot, therefore, be compared with them.

Moreover the "problem" given in the description (page 1, lines 17 to 23) must be considered to be a detailed version of the said general problem and indicates the direction of the possible solution. In the given technical field, however, which is characterised by a complex computer architecture and wherein a great number of different data transfers are possible, already an indication (of a disadvantage) that makes it possible to improve the function of the system, could contribute to the inventive step. In the present case the Board is of the opinion that the said detailed version of the problem can only support the inventive step, as it indicates a disadvantage in the function of the old system, which disadvantage has been successfully removed from the said system by the solution according to the sole claim.

4. It follows that the sole claim is allowable under Article 52(1) EPC.

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent in accordance with the Appellant's request (paragraph IV above).

The Registrar: The Chairman

M. Kiehl P.K.J. van den Berg