BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS | BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE | CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

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Application No.: 83 101 979.9

Publication No.: 0 088 338

Title of invention: Inverter device using gate turn-off thyristors

Classification: H02M7/48

D E C I S I O N
of 21 June 1991

Proprietor of the patent: Hitachi, Ltd.

Opponent: Siemens Aktiengesellschaft, Berlin und München

Headword:

EPC Article 56

Keyword: "inventive step - no"

Headnote

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number : T 356/90 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 21 June 1991

Appellant : (Opponent)
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Decision under appeal :
Interlocutory decision of the Opposition Division of the European Patent Office dated 12.04.90 concerning maintenance of European patent No. 0 088 338 in amended form.

Composition of the Board :

Chairman : R.E. Persson
Members : W.J.L. Wheeler
A. Hagenbucher

Summary of Facts and Submissions

I. European patent No. 88 338 was opposed by the Appellant on the ground that its subject-matter was not patentable within the terms of Articles 52 to 57 EPC.

II. The following documents, inter alia, were considered in the proceedings before the Opposition Division:

Da: GB-A-1 371 418
Db: Control Engineering, May 1964, p. 95-99
Dc: Hoffmann, Stocker: "Thyristor-Handbuch", Siemens, 1976, p. 247-249
Dd: Heumann, Stumpe: "Thyristoren", Teubner Verlag, 1974, p. 41-47
De: DE-C-646 827
Dg: Hitachi Review, Vol. 31 (1982), No. 1, p. 23-27.

III. By an interlocutory decision dated 12 April 1990, the Opposition Division decided that the patent in suit could be maintained on the basis of Claims 1 to 4 as amended on 2 October 1987 and an amended description. The present appeal is directed against that decision.

IV. In reply to a communication pursuant to Article 11(2) of the Rules of Procedure of the Boards of Appeal, the Respondent filed on 14 May 1991 new Claims 1 to 4 and an amended description. Claims 1, 3 and 4 are worded as follows:

"1. An inverter device comprising an inverter unit (2) including

- a d.c.-power source (1),
- a plurality of groups of unit switching circuits

connected in parallel to the d.c.-power source and each of them having gate turn-off thyristors (GTO; 4,6; 5,7; 8,10; 9,11; 12,14; 13,15) connected in series with each other,
- feedback diodes (16-27) each connected anti-parallel to the respective gate turn-off thyristor (4-15),
- at least two a.c.-output terminals, wherein
- those unit switching circuits which are operated in the same phase constitute a group and are connected by centre-tapped current balancing reactors (34, 35, 36),

characterised in that

each unit switching circuit further includes

- snubber circuits (S4-S15) respectively connected in parallel to each gate turn-off thyristor, wherein
- the centre-tapped current balancing reactors (34, 35, 36) respectively are connected between the series nodes (A, B) of the thyristors of the respective groups and the output terminals (U, V, W) are respectively led out from the centre point (O) of the centre-tapped current balancing reactors, thereby reducing the required capacitance in the snubber circuit.

3. An inverter device comprising

- a d.c.-power source (7),
- a plurality of groups of unit switching circuits, being connected in parallel to the d.c.-power source (7) and each of them having gate turn-off thyristors (4,6; 5,7; 45,47; 46,48) connected in series with each other,
- feedback diodes (16, 17, 18, 19, 49, 50, 51, 52) connected anti-parallel to the gate turn-off thyristors,

- a plurality of first centre-tapped current balancing reactors (34, 53) each of them connecting two unit switching circuits operating in the same phase,
- an a.c.-output-terminal,

characterised in that

- respectively four unit switching circuits constitute a group and are operated in the same phase,
- a snubber circuit (S4-S7, S45-S48) is respectively connected in parallel to each gate turn-off thyristor,
- the centre-tapped current balancing reactors are connected between the first and second one and between the third and fourth one of the four series nodes of the gate turn-off thyristors of each group,
- second centre-tapped current balancing reactors (54) are provided respectively connecting the centre points of the first reactors (34, 53) of the groups, wherein the a.c.-output-terminals are led out from the centre points of the second reactors,
- thereby reducing the required capacitance in the snubber circuit (Fig. 4).

4. An inverter device comprising a unit inverter (60, 62) being connected in parallel to at least a d.c.-power source (1; 63) and each having gate turn-off thyristors (4-15) connected in series with each other, feedback diodes (16-27) each connected anti-parallel to the respective gate turn-off thyristor (4-15) and a plurality of centre-tapped current balancing reactors (37, 38, 39) connecting thyristors operated in the same phase,

characterised in that

- a snubber circuit (S4-S15) is connected in parallel to each gate turn-off thyristor (4-15),

- a plurality of unit inverters being connected in parallel to at least a d.c.-power source are provided,
- the unit inverters are each connected with one another, and are separately connected to a d.c.-power source (1, 63),
- said reactors are respectively connected between the corresponding a.c.-output terminals of said respective unit inverters and having centre-taps to which respective phase terminals of a load (3) are connected, thereby reducing the required capacitance in the snubber circuit."

Claim 2 is dependent on Claim 1.

V. Oral proceedings were held on 16 May 1991. The Board reserved its decision.

VI. As far as inventive step was concerned, the Appellant argued in effect that the problem solved by the circuit configurations according to the contested patent was not that of reducing the capacitance required in the snubber circuits but rather the more modest one of how to combine the outputs of a plurality of GTO unit switching circuits (each comprising a series connection of two GTOs with associated feedback diodes and snubber circuits, the output being taken from the node between the GTOs, as was known per se) so as to increase the current capacity of the inverter system beyond that of an individual unit switching circuit. The idea of connecting the outputs of switching circuits in parallel through a centre-tapped current balancing inductance had been known for a long time, as may be seen from documents Da to De. Figure 6 of document Dg showed an inverter device having all the features specified in the prior art part of Claim 1 of the contested patent. Furthermore, it was clear from points (2) and (3) in the left hand column on page 27 of Dg that

the inverter device also included snubber circuits for the GTOs and a person skilled in the art would know that the snubber circuits would have to be connected in parallel with their respective GTOs. To a person skilled in the art confronted with the problem of combining the outputs of two GTO unit switching circuits it would be obvious to connect their outputs to respective ends of a centre-tapped current balancing inductance in the same way as was shown on page 97 of Db in respect of SCR circuits. There would be no need to modify the individual unit switching circuits. Thus, the claimed arrangements did not involve an inventive step.

VII. The Respondent argued in effect that the inverter devices according to the contested patent did make it possible to reduce the capacitance in the snubber circuits, compared with that required in the circuit shown in Figure 6 of Dg, where the snubber capacitors were in series with the leakage inductance of the current balancing reactor. The claimed arrangements were not obvious modifications of the inverter device shown in Figure 6 of Dg.

VIII. The Appellant requested that the decision under appeal be set aside and that the European patent No. 0 088 338 be revoked. An earlier request for reimbursement of the appeal fee was withdrawn.

IX. The Respondent requested that the patent be maintained on the basis of Claims 1 to 4 and the amended description as filed on 14 May 1991.

Reasons for the Decision

1. The appeal is admissible.

2. The main issue to be decided in the present case is whether or not the subject-matter of the contested patent involves an inventive step, taking into account the amendments proposed by the Respondent in the course of the appeal proceedings.

3. The parties consider the present case from two entirely different standpoints. The Proprietor (Respondent) argues that the subject-matter of the contested patent should be regarded as a non-obvious modification of the inverter shown in Figure 6 of Dg, in particular of the arrangement of the current balancing reactors, allowing a reduction in the capacitance required in the snubber circuits. On the other hand, the Appellant regards the subject-matter of the contested patent as an obvious solution of the problem of combining the outputs of a plurality of GTO inverters to obtain an inverter system with a current capacity greater than that of an individual GTO inverter.

4. It appears to the Board that the Appellant is correct in asserting that it is a common practice to combine the outputs of thyristors by means of centre-tapped current balancing reactors or balancing transformers to obtain a current capacity in excess of that of an individual thyristor (see, for example, Dd, page 45, and Db, whole paper). The Board notes that Db refers to dc-to-ac inverters in the second paragraph on page 95. In the opinion of the Board, Db, read as a whole by a person skilled in the art, clearly recommends the use of balancing transformers to combine and balance the output currents of paralleled SCRs (which are thyristors) in general, and in dc-to-ac inverters in particular.

5. As is acknowledged in column 1 of the contested patent, it belongs to the general knowledge of a person skilled in the art to protect a thyristor from excessive voltage by

shunting it with a "snubber circuit" consisting of a capacitor in series with a parallel connection of a resistor and a diode. This has not been disputed by the Respondent.

6. Document Dg discloses and recommends the use of gate turn-off thyristors (GTO) in dc-to-ac inverter devices. This document supports the Appellant's assertion that the "unit switching circuit" comprising a series connection of two GTOs (4, 6) with associated snubbers (S4, S6) and feedback diodes (16, 18) connected as shown in Figure 1 of the contested patent was already known per se. This follows from the circuit diagram (b) in Figure 5 on page 25 of Dg, which shows the fundamental circuit of a GTO inverter as comprising a series connection of two GTOs (MTh), with a feedback diode (Dr) connected anti-parallel to each gate turn-off thyristor. The output is taken from the node between the GTOs. Although they are not shown in Figure 5 (or in Figure 6), it is understood that snubber circuits are provided in practice, as may be deduced from the references to them in points (2) and (3) in the left hand column on page 27 of Dg.

7. In practice, the need frequently arises for dc-to-ac inverter circuits which are capable of carrying more current than their individual switching components can carry. In the opinion of the Board, it would be obvious to a person skilled in the art, who had to design a GTO dc-to-ac inverter having a current capacity greater than that of an individual GTO unit switching circuit (of the type shown in diagram (b) in Figure 5 of Dg including snubbers), to provide two (or more) of the known GTO unit switching circuits in parallel for each phase of the inverter and combine their outputs by means of current balancing transformers or centre-tapped current balancing

reactors, as taught by Db and Dd in respect of SCR circuits.

8. It seems to the Board that, in the course of pursuing this obvious line of action, the person skilled in the art would inevitably arrive at an inverter device having all the features specified in Claim 1 of the contested patent (see paragraph IV above). The fact that the capacitance required in the snubber circuits is less than that needed in the inverter arrangement shown in Figure 6 of Dg is a consequence of the obvious measures taken to increase the current capacity of the inverter, and cannot render these measures unobvious (in line with the decision in case T 21/81, OJ EPO, 1983, 15).

9. The Board therefore agrees with the Appellant that the subject-matter of Claim 1 does not involve an inventive step within the meaning of Article 56 EPC. It may be mentioned in passing that the same applies to the subject-matter of Claim 4 (insofar as it can be understood) and to that of Claim 3, which results when four of the known GTO unit switching circuits are provided for each phase of the inverter and their outputs combined by means of current balancing transformers or centre-tapped current balancing reactors, as taught by Db and Dd.

10. In the result, the Board is of the opinion that ground (a) in Article 100 EPC prejudices maintenance of the patent in suit in the amended form requested by the Respondent.

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.

2. European patent No. 0 088 338 is revoked.

The Registrar

M. Beer

The Chairman

E. Persson

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