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Application No.: 86 113 146.4  
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Title of invention: Sample-and-hold circuit

Classification: G11C 27/02

**D E C I S I O N**  
of 31 January 1991

Applicant: Kabushiki Kaisha Toshiba, et al  
Proprietor of the patent:  
Opponent:

Headword:

EPC Article 56

Keyword: "Inventive step (no)"

**Headnote**



Case Number : T 436/90 - 3.5.1

**D E C I S I O N**  
**of the Technical Board of Appeal 3.5.1**  
**of 31 January 1991**

**Appellant :**

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**Decision under appeal :**

Decision of Examining Division of the European  
Patent Office dated 28 February 1990 refusing  
European patent application No. 86 113 146.4  
Article 97(1) EPC.

**Composition of the Board :**

**Chairman :** P.K.J. van den Berg  
**Members :** A.S. Clelland  
F. Benussi

**Summary of Facts and Submissions**

I. Appellant's European patent application No. 86 113 146.4, filed on 24 September 1986, claiming priority from a previous application in Japan dated 30 September 1985, was refused by a decision of the Examining Division dated 28 February 1990.

II. The reason given for the refusal was that the subject-matter of each of the claims lacked an inventive step having regard to the prior art known from the following documents:

D1: IEEE Journal of Solid-State Circuits, Vol. SC-18, No. 6, December 1983, New York, USA, pages 716-722, VAN DE PLASSCHE et al.: "A monolithic High-Speed Sample-and-Hold Amplifier for Digital Audio";

D2: US-A-4 365 204;

D3: IEEE Journal of Solid-State Circuits, Vol. SC-12, No. 6, December 1977, New York, USA, pages 592-599, CAVES et al.: "Sampled Analog Filtering Using Switched Capacitors as Resistor Equivalents";

III. On 26 April 1990 the Appellant filed a notice of appeal against the above decision, together with the appeal fee. A statement setting out the grounds of appeal was subsequently filed on 15 May 1990, together with new claims to replace those previously on file.

IV. In a communication pursuant to Article 11(2) of the Rules of Procedure of the Boards of Appeal, the Board discussed D1 and the following additional documents:

- D4: IEEE International Solid-State Circuits Conference, Vol. 27, February 1984, New York, USA, pages 120-121, SATO et al.: "A CMOS CCD Video Delay Line".
- D5: "Switched Capacitor Circuits", Allen and Sanches-Sinencio, Van Nostrand, New York 1984, pages 1, 94-101, 117, 382, 442, 559, 608, 609, 639 and 640;
- D6: "Digital Signal Processing", ed. N.B. Jones, Peter Peregrinus Ltd., UK 1982, pages 122,123;
- D7: IEEE Custom Integrated Circuits Conference 1989, pages 6.5.1 to 6.5.4, SUGAWA et al.: "CMOS Low Distortion Sample & Hold Circuit for Audio D/A Converter.

- V. In response to the communication the Appellant, on 14 January 1991, filed new Claims 1, 2 and 7; he argued that the subject-matter of the independent Claims 1 and 2 was novel and inventive.
- VI. In oral proceedings held on 31 January 1991 the Appellant requested that
- the decision under appeal be set aside and a patent granted on the basis of:

**Claims**

Claims 1, 2 and 7 filed with the submission of 14 January 1991,

Claims 3 to 6 filed with the submission of 15 May 1990,

**Description**

pages 1, 5 and 6 as originally filed,  
pages 2 and 2a filed with the submission of 15 May 1990,  
pages 3, 4, 7 and 8 filed with the submission of  
14 January 1991,

**Drawings**

sheets 1/5 to 5/5 as originally filed.

VII. The application includes two independent claims, Claims 1 and 2. Claim 1 reads as follows:

"A sample-and-hold circuit comprising:

- impedance-converting means (16) including a unity gain amplifier;
- first switching means (S5);
- amplifying means (17);
- input means (15) having an input node for receiving an input signal and supplying an output signal corresponding to the input signal to the amplifying means (17) through the impedance-converting means (16) and the first switching means (S5);
- output-holding capacitor means (CH) coupled between the input and output terminals of the amplifying means (17); and
- feedback means (18) coupled between the output terminal of the amplifying means (17) and the input terminal of the impedance-converting means (16), characterized in that
- said input means (15) is constituted of a first switched capacitor unit (15) including a first capacitor (C1), second switching means (S11, S12) for coupling one electrode of said first capacitor (C1) to said input node, and the other electrode of said first capacitor (C1) to the input terminal of said impedance-converting means (16) in accordance with a first control signal

- ( $\phi 1$ ), and a third switching means (S21, S22) for coupling one electrode of said first capacitor (C1) to a first voltage terminal, and the other electrode of said first capacitor (C1) to a second voltage terminal in accordance with a second control signal ( $\phi 2$ ), said second switching means (S11, S12) being turned on after said third switching means (S21, S22) are turned off, and said third switching means (S21, S22) being turned on after said second switching means S11, S12) are turned off,
- said feedback means (18) is constituted of a second switched capacitor unit (18) including a second capacitor (C2), a fourth switching means (S13, S14) for coupling one electrode of said second capacitor (C2) to the input terminal of said impedance-converting means (16), and the other electrode of said second capacitor (C2) to the output terminal of said amplifying means (17) in accordance with said first control signal ( $\phi 1$ ), and a fifth switching means (S23, S24) for coupling one electrode of said second capacitor (C2) to the first voltage terminal, and the other electrode of said second capacitor (C2) to the second voltage terminal in accordance with said second control signal ( $\phi 2$ ), said fourth switching means (S13, S14) being turned on after said fifth switching means (S23, S24) are turned off, and said fifth switching means (S23, S24) being turned on after said fourth switching means (S13, S14) are turned off,
  - said impedance-converting means (16) being a source follower circuit having a first MOS transistor (Q1;Q4) whose gate receives an output signal (V1) from said first switched capacitor (15), and a second MOS transistor (Q2;Q3) which is coupled in series to the first MOS transistor (Q1;Q4) and whose gate receives a predetermined voltage ( $V_B$ ), and

- said first switching means (S5) being controlled by a third control signal ( $\phi_3$ ), and being turned on a predetermined period of time after said second and fourth switching means (S11, S12 and S13, S14) are turned on, and said second and fourth switching means (S11, S12 and S13, S14) being turned off a predetermined period of time after said first switching means (S5) is turned off (Fig. 5)."

VIII. Claim 2 has the same preamble as Claim 1 and includes in its characterising part the following features:

- "- said input means (15) is constituted of a first switched capacitor unit (15) including a first capacitor (C1), second switching means (S11, S12) for coupling one electrode of said first capacitor (C1) to ground, and the other electrode of said first capacitor (C1) to the input terminal of said impedance-converting means (16) in accordance with a first control signal ( $\phi_1$ ), and a third switching means (S21, S22) for coupling one electrode of said first capacitor (C1) to said input node, and the other electrode of said capacitor (C1) to ground in accordance with a second control signal ( $\phi_2$ ), said second switching means (S11, S12) being turned on after said third switching means (S21, S22) are turned off, and said third switching means (S21, S22) being turned on after said second switching means (S11, S12) are turned off,
- said feedback means (18) being constituted of a second switching capacitor unit (18) including a second capacitor (C2), a fourth switching means (S13, S14) for coupling one electrode of said second capacitor (C2) to the input terminal of said impedance-converting means (16), and the other electrode of said second capacitor (C2) to the output terminal of said amplifying means (17) in accordance with said first control signal ( $\phi_1$ ),

and a fifth switching means (S23, S24) for coupling one electrode of said second capacitor (C2) to ground, and the other electrode of said second capacitor (C2) to ground in accordance with said second control signal ( $\phi 2$ ), said fourth switching means (S13, S14) being turned on after said fifth switching means (S23, S24) are turned off, and said fifth switching means (S23, S24) being turned on after said fourth switching means (S13, S14) are turned off,"

The remaining features of the characterising part correspond to the last 15 lines of Claim 1, i.e. the impedance-converting means and control of the first switching means, reference being made in the last line of the claim to Fig. 9.

#### Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is, therefore, admissible.
2. The amendments made to the application documents do not contravene Article 123(2) or (3) EPC and are, therefore, also admissible.
3. The application is explicitly concerned with an improvement in the sample-and-hold amplifier circuit disclosed at Figure 1 of D1. This known arrangement has disadvantages arising from the use of the two resistors R. The use of these resistors provides a potential path for coupling between the input and output of the circuit by means of which performance could be degraded; to overcome this the common point of the resistors is shorted to earth by switch S<sub>1</sub> except when sampling is taking place, i.e. when switch S<sub>2</sub> is closed. Even so, the use of the

resistors requires that the output of the circuit being sampled be of much lower impedance than the resistance of the left-hand resistor R, or conversely, that the resistance R be increased in value to be much higher than this output impedance. According to information supplied by the Appellant such high resistance is difficult to fabricate using integrated circuit techniques.

Furthermore, during sampling when the switch  $S_1$  is connected to the first, unity gain, operational amplifier  $A_1$ , coupling will still occur between the input and output of the circuit by way of the right-hand resistor R.

4. The means by which in accordance with Claims 1 and 2 these problems are overcome may be summarised as follows:

(a) Replacement of both the resistors R by switched-capacitor units. Two alternative units are described in the application, the arrangement of Figure 5 being claimed in Claim 1 and that of Figure 9 in Claim 2.

(b) The unity-gain amplifier,  $A_1$  in Figure 1 of D1, is constituted by a source follower circuit formed of MOS transistors.

(c) The switching of the sample-and-hold switch is controlled to take place during a predetermined portion of the control cycle of the switches of the switched capacitor units.

The claimed arrangements do not require the presence of a shorting switch such as switch  $S_1$  shown in Figure 1 of D1.

5. Claims 1 and 2 are correctly delimited with respect to D1. No other single document discussed in the proceedings discloses the features of a sample-and-hold circuit of the

kind shown in D1 which goes beyond this disclosure and Claims 1 and 2 are each accordingly novel.

6. Turning now to inventive step, the Board accepts that the correct starting point for considering the claimed invention is the circuit shown at Figure 1 of D1.

In the view of the Board the object of the invention given above should be amplified to include the implementation of the improved sample-and-hold circuit in monolithic MOS integrated circuit technology. D1 is directed to a monolithic integrated circuit but makes use of bipolar rather than MOS technology, see the paragraph bridging the left and right-hand columns of page 720 of D1. The description of the application implies but does not explicitly state that the disclosed circuits are implemented as integrated circuits, page 5, line 4 referring to "pattern area"; the applicant acknowledges this in the submission of 12 May 1989 at page 4, second full paragraph, as well as in the submission of 15 May 1990 at page 4, second paragraph. It is therefore clear that the claimed invention is to be implemented in monolithic integrated circuit technology.

That MOS - rather than bipolar - technology is involved appears from the use in Figures 10 and 11 of MOS transistors and from the submission to the Examining Division dated 29 December 1989. This refers to document D7, a paper presented by two of the inventors named in the present application at the IEEE Custom Integrated Circuits Conference; the paper is explicitly concerned with monolithic MOS technology and is stated to disclose "a circuit arrangement which is very similar to that disclosed in Figure 5 of the present application".

7. It has not been contested by the Appellant - see the submission of 12 May 1989 at page 6, first full paragraph - that the skilled man implementing the circuit of Figure 1 of D1 would find it obvious to use switched-capacitor units to avoid the necessity of fabricating high-value resistors. Switched-capacitor units are generally implemented in MOS technology. Referring to D6, part 7.2.5 last paragraph: "the main attraction of SC [switched-capacitor] filters is their integrated circuit realisation using MOS techniques to produce realisable complete systems on a single chip". D5, which is a university textbook, indicates in the introduction at page 1 that MOS technology is particularly appropriate to sampled data signal processing, of which the switched-capacitor filter is an example. According to page 559 of D5 an extremely close relationship exists between switched-capacitor filter design and MOS technology, and "MOS technology is typically selected for switched-capacitor circuit implementation".
  
8. The skilled man is thus led to implement the D1 circuit with switched-capacitor filters using MOS technology. Once he has taken this step the subject-matter of each of Claims 1 and 2 follows directly from an application of the common general knowledge in the art, as exemplified by documents D4, D5 and D6, to the circuit of Figure 1 of D1.

Looking at the actual embodiments of the invention, Figure 5 - to which Claim 1 is directed - makes use of the switched-capacitor arrangement referred to in connection with Figure 2.5-8(b) of D5 at page 98 as a "series SC inverting integrator". The Figure 9 embodiment, to which Claim 2 is directed, makes use of the "non-inverting parallel SC integrator" switched-capacitor arrangement shown at Figure 2.5-5 at page 94. These switching

arrangements and their characteristics are so well known as to be referred to elsewhere in the text as "building blocks" and are illustrated in tabular form at page 95. An example of the combination of two of these "building blocks" with the same switching cycles as in Figure 9 is given in Figure 2.6-10 at page 117, whilst Figure 5.3-1 at page 382 shows the application of one of the above-mentioned "building blocks" to a sample-and-hold arrangement.

It would accordingly be obvious for the skilled man implementing the Figure 1 circuit of D1 using switched-capacitor filters, to use any of the "building blocks" disclosed by D5 in any suitable combination.

The use of non-overlapping clocks as a prerequisite for switched-capacitor circuit operation is discussed at pages 608 and 609 of D5 and at page 122 of D6.

The source follower as a useful tool of MOS technology for providing a low output resistance is discussed in D5 at pages 639 and 640 and its application to sample-and-hold circuits is explicitly shown in D4, in which the application is that of impedance transformation. It would thus be clear to the skilled man that in implementing the D1 circuit in MOS technology he could make use of a source follower as impedance converting means in place of the amplifier A<sub>1</sub>.

9. Accordingly, all the features of each of Claims 1 and 2 follow as a matter of course once the skilled man decides to implement Figure 1 of D1 in MOS monolithic integrated circuit technology. The subject-matter of each of these claims therefore lacks an inventive step.

10. Against the above analysis the Appellant has advanced the following arguments:

- (1) The particular combinations of features claimed in Claims 1 and 2 are not known from, or derivable in a non-inventive manner from, the prior art.
- (2) The Figure 1 arrangement of D1 makes use of a shorting switch which serves to short the input to the first stage at all times other than the sampling period; by means of this switch coupling between the input and output of the circuit is prevented. Even if the skilled man were to replace the resistors of D1 by switched-capacitor units he would not dispense with this switch.
- (3) The skilled man, even if he were to replace the resistors in D1 by switched-capacitor units, would not provide a circuit having the claimed specific timing relationships for on the one hand the various switches of the switched-capacitor units and on the other hand the sample-and-hold switch.

11. Dealing with each of these points in turn, it has already been observed that the use of MOS technology has particular advantages in the context of sample-and-hold circuitry, so that the skilled man would, in implementing the Figure 1 circuit of D1, be led to use MOS technology. From the use of such technology follows the substitution of switched-capacitor units for the resistors used in the D1 circuit and the use of a source follower circuit as impedance-converting means. Although MOS technology is not explicitly a feature of Claims 1 and 2, once the step to use it is taken then merely by an application of the common general knowledge of the man skilled in the art the circuit arrangements of Figures 1 and 2 are arrived at.

12. As regards point 2, the use of switched-capacitor units clearly obviates the need for any shorting switch at the input of the impedance-converting stage and the skilled man would therefore, as a matter of course, eliminate the switch.
  
13. As regards the specific timing relationships between the various switches, it is self-evident that the switched-capacitor units only require two timing signals; Figure 2.6-10 of D5, referred to above, is an example of the combination of two switched-capacitor units in which only two timing signals are provided. It is also self-evident that sampling cannot be undertaken during a transition period since the switches are controlled by non-overlapping clocks.

Since Claims 1 and 2 are not allowable, the dependent Claims 3 to 7 must share the same fate. In any case, these claims do not add any inventive feature to either Claim 1 or Claim 2.

**Order**

**For these reasons, it is decided that:**

The appeal is dismissed.

The Registrar:

The Chairman:

M. Kiehl

P.K.J. van den Berg