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File Number: T 478/90 - 3.5.1

Application No.: 83 900 515.4

Publication No.: 0 112 337

Title of invention:

Classification: H04L11/20

D E C I S I O N  
of 3 February 1992

Proprietor of the patent: Western Electric Company, Incorporated

Opponent: Standard Elektrik Lorenz AG

Headword:

EPC Article 56

Keyword: "Inventive step (yes)"

Headnote



Case Number : T 478/90 - 3.5.1

**D E C I S I O N**  
of the Technical Board of Appeal 3.5.1  
of 3 February 1992

**Appellant :**  
(Proprietor of the patent)

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**Decision under appeal :**

Decision of Opposition Division of the European  
Patent Office dated 11 April 1990 revoking  
European patent No. 0 112 337 pursuant to  
Article 102(1) EPC.

**Composition of the Board :**

**Chairman :** Van den Berg P.K.J.  
**Members :** Clelland A.S.  
Schar-Schuppisser M.W.

**Summary of facts and submissions**

- I. European patent No. 0 112 337 claiming priority date of 25 June 1982 was granted on 2 March 1988 on the basis of European patent application 83 900 515.4, filed on 12 January 1983.
- II. An opposition was filed on 30 November 1988 on the grounds that the subject-matter of the patent did not fulfil the requirements of Articles 54 to 57 EPC.

The Opponent referred to the prior art documents:

- D1: Electrical Communication Vol 56, No 1, 1981, pages 44 to 56
- D2: Electrical Communication Vol 56, No 2/3, 1981, pages 114 to 125
- D3: Electrical Communication Vol 56, No 2/3, 1981, pages 148 to 160
- D4: Electrical Communication Vol 56, No 2/3, 1981, pages 264 to 273
- D5: IEEE Transactions on Computers, Vol C-28, No 10, October 1979, pages 699 to 703, A.Hopper et al. "Binary Routing Networks"

D1 to D4 were published in both German and English, the German version having initially been cited by the opponent but the above-mentioned English equivalents having been considered in both the opposition and the present proceedings.

- III. By its decision of 11 April 1990 the Opposition Division revoked the patent.

IV. On 8 June 1990 the patent proprietor (Appellant) lodged an appeal against this decision, the prescribed appeal fee having been paid on 6 June 1990. In the Grounds of Appeal, filed on 11 August 1990, the Appellant requested that the decision of the Opposition Division be set aside and that the patent be maintained on the basis of Claims 1 to 5 filed the same day.

V. On 19 August 1991 the Appellant deleted Claim 5 and filed as an auxiliary request auxiliary Claims 1 to 3.

VI. Claim 1 as filed on 11 August 1990 reads:

"1. A fast packet switching system for switching packets for a plurality of messages from a plurality of transmission links comprising a packet switching network (116) having a plurality of interconnected packet switch nodes (500-15), and CHARACTERISED BY a plurality of distributed controllers (131) each for interfacingly connecting an individual one of said transmission links (132) to one of said packet switch nodes (500-15) and comprising memory means (1401) for storing translation information for controlling the routing of packets of one of said messages communicated over said one of said links through a plurality of said switch nodes to another of said controllers (130), and means (1404) responsive to translation information stored in said memory means to produce a plurality of address bits for concatenating said plurality of address bits with each of said packets of said one of said messages, said one of said switch nodes (500-15) comprising a plurality of input conductors (515, 519, 520, 521), a plurality of output conductors (522, 523, 524, 516), input control means (1000) responsive to a predetermined number of said concatenated plurality of address bits from one of said input conductors (515) for routing a received packet of said one of said messages with received concatenated plurality of address bits from

said one of said input conductors (515) to a particular one of said output conductors (516) defined by said predetermined number of address bits, and address rotation circuitry (1106) for repositioning said predetermined number of address bits in said received concatenated plurality of address bits in the routing of said received packet with received concatenated plurality of address bits to said defined one of said output conductors (522)."

VII. In a communication pursuant to Article 11(2) of the Rules of Procedure of the Boards of Appeal dated 12 December 1991 the Rapporteur commented on the documents on which the Opponent principally relied, namely D1 to D5, as well as other prior art regarded as relevant, in particular

D6: Proceedings of IEE, Vol 119, No 12, 1972, pages 1677 to 1682, Beeforth et al., "Proposed organisation for packet-switched data-communication network".

VIII. Oral Proceedings were held on 3 February 1992.

The Appellant's arguments in support of the patentability of the subject-matter of Claim 1 can be summarised as follows:

The cited documents D1 to D4, referring to the Respondent's "System 12", could not render the subject-matter of Claim 1 obvious since they did not disclose true packet switching, but rather a form of circuit switching. A path is set up through the switching network by means of so-called select commands, but these commands are not concatenated with each packet. Instead, once the path has been established every packet along the path (in a specified time slot, since "System 12" is a time-multiplexed system) will be directed the same way.

IX. The Respondent argued that although the system described in D1 to D4 functioned in a circuit switching mode, the system design is in fact such as to lend itself to the implementation of packet switching. Furthermore, the method of setting up a path as described in D1 to D4 involves concatenation of an address part with a data part since the "select" commands can be seen as a header associated with, if not immediately attached to, the following data packets. The close relationship between the "select" commands and the data is accentuated by the fact the commands are not separately acknowledged by the system.

The Respondent also mentioned D5 which was said to disclose packet switching as well as address rotation. It would not be necessary that the packets contained the complete address needed to transit the system; they could carry the address for just a part of the path ("Teilstreckenvermittlung").

X. The Appellant requested the maintenance of the patent on the basis of the following documents:

Claims:           1 to 4 filed on 11 August 1990 (main request)  
                  1 to 3 filed on 19 August 1991 (auxiliary request)

Description:      Pages 3 to 24 as granted, with page 4, lines 7 to 24, replaced by the content of page 4a as received on 13 May 1989 (both requests)

Drawings:         As granted (both requests)

XI. The Respondent requested that the appeal be dismissed.

### Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is, therefore, admissible.
2. The amendments made to the patent are also admissible. The only substantive amendments are those to Claim 1. The amendments were made so as to more clearly distinguish the claimed subject-matter from the cited prior art; all the features of the originally filed and the granted claims can be identified. Articles 123(2) and (3) EPC are accordingly met.
3. Since the Board finds that the main request is allowable, it has not proved necessary to consider the auxiliary request.
4. Claim 1 is directed to a "fast" packet switching system. The Patentee argued that "fast" meant more than the standard 64 kbit/s ISDN data rate and pointed to the statement at page 3 lines 44 to 55 of the granted patent, in which various disadvantages of the 64 kbit/s data rate as used in the prior art are stated. A figure of 8 Mbit/s is mentioned in the patent at page 4 line 64 as the desired data rate.

However, the claim contains no specific technical features which define what is meant by "fast"; viewed from the perspective of telephone exchanges in use at the claimed priority date, a 64 kbit/s data rate is "fast". The Board do not therefore consider that this relative term can serve to limit the scope of Claim 1 to systems substantially faster than 64 kbit/s and no weight has been given to the term in arriving at the present decision.

5. The Respondent has primarily relied on the documents identified above as D1 to D4, which show the early design of the ITT 1240 digital telephone exchange, referred to throughout the proceedings as "System 12". Although other documents relating to System 12 were referred to by both parties in the course of the proceedings, these either failed to cast any light on what was known before the claimed priority or added nothing to the disclosures of D1 to D4.

As regards System 12, therefore, only D1 to D4 are considered in the present decision.

6. It was considered by the Respondent that the System 12 exchange was at the priority date claimed for the patent suitable for use in packet switching and, if so used, would have given rise to a packet switching system which was "fast" in the sense of Claim 1, a 64-kbyte/s data rate being used, and which differed in substance from that claimed only in the use of addressing by means of "bit eating" rather than the claimed "bit rotation"; the Respondent further considered that it would have been obvious to the skilled man, given the disclosure of D5, to modify System 12 to introduce addressing by means of bit rotation.
7. It has accordingly been necessary to consider the structure of System 12 at the claimed priority date in some detail. Although described in D1 to D4, it is not always clear from reading these documents whether what is being described is operating hardware or a specification to be met at some future date. In the course of the oral proceedings the Respondent explained that the design of System 12 was essentially modular, so as to be

sufficiently flexible to accommodate future technical developments. The described exchange consists of a digital switching network (DSN) to which are connected a plurality of user and trunk modules (D1, Figure 2) including a packet user module (PUM). The digital switching network is primarily discussed in D3. From this document it can be seen that the DSN consists of a plurality of switching elements each comprising a plurality of switch ports and a time-multiplexed bus (Figure 1 at page 149). The switching elements make up four switching stages, namely stage 1 access switches and stages 2-4 group switches (Figure 3 at page 151). The input side of the switch ports can be seen from Figure 10 of D3 to include a "channel RAM" in which according to page 157, left hand column, path information is stored. Terminals are connected to the access switches by way of terminal interfaces of a terminal control element (page 150, right hand column). Path set up between two such terminal control elements was acknowledged by the Respondent to be by means of a free search up to the so-called "reflection point" and thereafter directed (D2 at page 122, right hand column, "Traffic Handling" and D3 at page 153, right hand column). According to D3 at page 149 right hand column, the step-by-step manner in which the switches make a connection is analogous to that of the older Strowger switches. In order to set up a path, a string of select commands is generated by the originating control element, each command establishing a connection in one switching element; a return path is set up independently using the select commands by the destination control element (page 153, left hand column). These commands are only issued when a call is initiated and thereafter so-called spata (speech or data) words can be sent. The connection is maintained until two successive

idle commands are sent (page 154, right hand column). From pages 155 to 157 it can be seen that the (synchronous) data format provides data words which do not contain address information; depending on the protocol bits each word defines either data or an address, but never both. System 12 thus sets up a virtual circuit (virtual in view of the time multiplexing) which is maintained until receipt of commands breaking the circuit; any subsequent connection between the same two terminals will not be constrained to follow the same path.

8. Turning now to the modules connected to the DSN, these are said to "incorporate hardware-identical TCEs (terminal control elements) ...they communicate over the digital switching network via a standardised interface" (D2 at page 119). According to D1, page 47, the packet user module "concentrates user traffic onto 64 kbit s-1 channels ...and operates the internal links (via the digital switching network) from locally terminated packet subscribers ...to the packet network". According to page 48 of D1 the PUM "provides access to a dedicated packet switched data network for ...packet users via trunk circuits ...its primary functions are to support a semipermanent link to the packet network...". At page 49, Table 2(b), for the class of connection "Data call between packet terminals" the switching module is said to be "PUM-PUM" and the connection type is said to be "packet switched"; however, from page 50 it appears that packet switching is only used within the packet user modules, the DSN providing "semipermanent paths" between the PUM and the packet network. This is confirmed by pages 53 and 54, which in connection with Figure 10 indicate that a separate packet switched node is provided, the DSN providing "semipermanent and circuit switched connections". Page 121 states that "Because control elements operate through a standard interface, new

terminal types can be added or existing ones modified without affecting the digital switching network or other modules."

9. In contrast to System 12, which as shown above is circuit-switched, the patent is explicitly concerned with a packet switching system. The expression "packet switching" is used in the art to indicate a digital data communication system in which the individual data words or packets contain address information which is used to control switching nodes through which the packets are sent and thus to steer them through the network. The form of packet switching used in the patent does not provide each packet with all the address information needed to transit the switching network but initially sets up a path using distributed controllers associated with the trunk or transmission links, each controller being equipped with a memory containing a translation table; the address contained in the incoming trunk packet is compared with the memory contents and translated into a new address which is concatenated with the packet. In passing through a switch node the concatenated address is subjected to bit rotation in order to facilitate routing through the node. In the preferred embodiment each switching network (Figure 5) contains paths with three successive switching nodes (Figure 10) each containing address rotation circuitry (Figure 11). The transmission link controllers (trunk controllers, Figure 14) thus modify the trunk packets to include address bits defining three successive addresses (Figures 6 to 9).
  
10. In Claim 1 a packet switching system is claimed which includes a plurality of distributed controllers containing memory means which store translation information for controlling the routing of packets, i.e. address information. Although the switch ports of System 12

include a "channel RAM" which can be viewed as a distributed controller, the purpose of this RAM appears to be to store the addresses for the respective time slots rather than translation information. The claim furthermore specifies that this translation information is used to produce a plurality of address bits which are concatenated with packets, these address bits being used at the switch nodes to route each packet along a path defined by a predetermined number of the address bits. This implies that address information on the incoming packets is translated, so that an incoming packet with a particular trunk address will always follow the same path to its destination, the path being determined by the incoming address and the information in memory. A packet entering a node on one input line will not automatically exit on the same output line as every other packet but on a line determined by the concatenated address. This is to be distinguished from circuit switching as used in System 12, in which the data will always follow the path determined by the set up select commands.

11. In the course of the oral proceedings the Respondent argued that even if, as described in D1 to D4, System 12 did not disclose the use of packet switching in the manner claimed, it was in fact prepared for such a use. If the skilled man were faced with the problem of modifying System 12 to provide packet switching he would make use of the disclosure of D5 so as to provide, in a non-inventive manner, the claimed system.
  
12. D5 discloses a system intended for a computer local area network. The routing nodes are switches controllable by the packet addresses and there are no "distributed controllers" in the sense of the claim: although buffers are provided at the nodes, these are not memory means for storing translation information for controlling the

routing of packets as required by claim 1. D5 provides packet switching by means of routing bits which are rotated as they pass one routing node so as to provide a new address at the next node. At page 701, left hand column, it is stated that "the route field is wide enough to steer packets to every part of the system", i.e., there is no need for the concatenation of address bits with the packets. In a modification of the main disclosure, D5 refers at page 701, left hand column, to "a translator, to change destinations into bits for steering... in such a case dynamic routing is easily implemented". Page 703, left hand column, states that "addressing has to be relative rather than absolute".

13. The Board are unable to see why the skilled man would feel a need to adapt System 12 to packet switching. As described, System 12 permits packet switching by way of packet user modules and the circuit-switched connections provided by the switching network; it also permits many other kinds of data transfer. Modifying the switching network to make use of packet switching would seem to conflict with the time multiplexed nature of this network and to reduce its flexibility. A combination of System 12 with the disclosure of D5 thus appears contrived and artificial. Moreover, even if for the sake of argument the skilled man were to adapt System 12 to packet switching by making use of the teaching of D5, he would not arrive at the claimed arrangement. The obvious adaptation would be to provide full addressing at the terminal control elements to take each packet through the entire digital switching network. Such an arrangement dispenses with the need for a preliminary route set up as used in the preferred embodiment of the patent and avoids the need for a memory for storing translation information for enabling the packet to pass through each switch node.

14. Nor does the modification of the D5 arrangement employing "a translator, to change destinations into bits for steering" lead in combination with the System 12 disclosure to the claimed subject-matter. The subsequent passage in the text of D5 states that use of a "translator" is "at the expense of a route field delay, since the entire field has to be absorbed before emitting". This modification is not wholly clear to the Board but must apparently be read in conjunction with the comment at page 703, left hand column, that "addressing has to be relative rather than absolute". It thus appears that this is an alternative to relative addressing by means of bit rotation, which is said at page 699, right hand column to give a delay of "only one or two bits rather than the entire routing field". The modification thus dispenses with bit rotation and leads away from the claimed system.
15. Finally, the Board consider that the skilled man, faced with the patentee's objective of a "fast" packet switching system, would find it not obvious to use the address rotation of D5 in the packet switching system of D6. D6 was not addressed by the Respondent but has been considered by the Board, exercising its discretion under Article 114(1) EPC. The document discloses a packet switching system in which trunk lines or transmission links are connected by way of input and output terminal units to a control processor forming a switching node. A route through the system is set up by means of a route search packet which at each exchange or node is used to compile a route list. All message packets follow the route which has been set up. In consequence, each packet need not hold the complete destination address but can be given an abbreviated address. D6 does not disclose the manner in which switching is effected at the nodes and assumes throughout that the abbreviated address is sufficient to

ensure switching through the system. No details are given of how the control processor operates. The terminal units can be viewed as processors in that they connect transmission links to the switch node, but they perform only housekeeping functions such as identifying packet type, identifying packet start/end, CRC checks and link synchronisation.

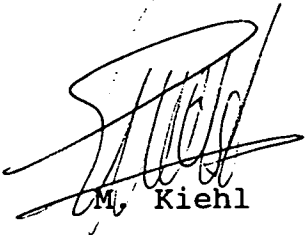
15. The use of bit rotation in the system of D6 does not appear to the Board to be an obvious modification to make; it only commends itself with the benefit of hindsight. Even if, for the sake of argument, bit rotation were to be incorporated in the system of D6, the obvious manner of doing so would be to provide a packet header of sufficient length to accommodate all address information needed to transit the system. Such a combination would not require controllers having memory means for storing translation information or means to produce a plurality of address bits for concatenating with each of the packets. Thus, the combination would not result in the claimed system.
  
17. For these reasons, in the Board's view, the subject-matter of Claim 1 of the main request involves an inventive step.
  
18. Claim 1 being allowable, the same applies mutatis mutandis to dependent Claims 2 to 4, which relate to specific embodiments of the packet switching system of Claim 1.

**Order**

**For these reasons, it is decided that:**


1. The appeal is allowed.
  
2. The case is remitted to the first instance with the order to maintain the patent on the basis of the claims of the main request specified at paragraph X above.

The Registrar



M. Kiehl

The Chairman



P.K.J. Van der Berg