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Bezeichnung der Erfindung: Sample and hold circuit
Title of invention:
Titre de l'invention :

Klassifikation / Classification / Classement : G11C 27/02

ENTSCHEIDUNG / DECISION

vom / of / du 15 November 1990

Anmelder / Applicant / Demandeur : KABUSHIKI KAISHA TOSHIBA

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Article 56

Schlagwort / Keyword / Mot clé : "Inventive step (yes)"

Leitsatz / Headnote / Sommaire

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Case Number : T 550/90 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal
of 15 November 1990

Appellant : KABUSHIKI KAISHA TOSHIBA
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Decision under appeal : Decision of Examining Division 2210 of the European Patent Office dated 26 February 1990 refusing European patent application No. 84 113 302.8 pursuant to Article 97(1) EPC.

Composition of the Board :

Chairman : P. van den Berg
Members : R. Randes
M. Lewenton

Summary of Facts and Submissions

I. European patent application No. 84 113 302.8 (publication No. 0 144 759), claiming a priority as from 11 November 1983, based on a prior application in Japan and filed on 5 November 1984, was refused by decision of Examining Division 2.2.10.067 dated 26 February 1990.

II. That decision was based on the ground that the subject-matter of Claims 1 to 4 filed on 28 June 1989 was not considered to involve an inventive step with respect to the prior art disclosed in the following documents:

D1: US-A-3 412 263

D3: IEEE TRANSACTIONS ON COMMUNICATIONS, Vol. COM-22, No. 7, July 1974, pages 986-994, New York, USA; G.M. BENSON: "Thin-Film Auto-Balance Diode Gate for Voice-Band Sample and Hold and Resampler Circuits".

D4: MIT Lincoln Laboratory Technical Report No.300, January 30, 1963, R.H. Baker et al.: "The Diamond Circuit".

III. The Appellant (Applicant) lodged a notice of appeal against this decision on 25 April 1990 and paid the relative fee on the same day. A statement of grounds was filed on 26 June 1990.

IV. The Appellant requests that the decision under Appeal be set aside and that a patent be granted on the basis of the following documents:

Claims:
Nos. 1 to 4 as filed on 28 June 1989;

Description:
Pages 3 and 9 as originally filed
Pages 1, 2, 4 and 5 to 8 as filed on 14 July 1987
Pages 4a and 4b as filed on 26 June 1990;

Drawings:
Sheets 1/3 to 3/3 as originally filed

V. Claim 1 reads as follows (with three clerical errors corrected - "und" at lines 2 and 4 in the second paragraph and at line 15 of the third paragraph of the characterising part changed into "and"):

"A sample and hold circuit comprising:

input and output terminals (IN, OUT);

first and second power source terminals;

capacitive means (C1) connected between said output terminal (OUT) and said second power source terminal;

a first transistor (Q10) of one conductivity type which has a collector connected to said first power source terminal and an emitter connected to said output terminal (OUT);

a second transistor (Q12) of the opposite conductivity type which has an emitter connected to said output terminal (OUT);

a third transistor (Q14) of the opposite conductivity type which has a base connected to said input terminal (IN), and an emitter connected to a base of said first transistor (Q10);

a fourth transistor (Q16) of the one conductivity type which has a base connected to said input terminal (IN), a collector connected to said first power source terminal, and an emitter connected to a base of said second transistor (Q12); and

a driving control circuit (38) including mode setting means (40) for selectively setting sampling and holding modes and current control means (Q18, Q20) to inhibit flow of the respective base currents of said first and second transistors (Q10, Q12) in the holding mode and to permit flow of the respective base currents of said first and second transistors (Q10, Q12) in the sampling mode;

characterized in that

said mode setting means includes a voltage generating circuit (40) which generates a first voltage (V1) at a high level and a second voltage (V2) at a low level from respective first and second control terminals during the sampling mode and generates the first voltage (V1) at a low level and the second voltage (V2) at a high level from the respective first and second control terminals during the holding mode,

said current control means includes first and second switching means (Q18, Q20), said first switching means (Q18) is connected between said first control terminal and the base of said first transistor (Q10), and said second switching means (Q20) is connected between said second control terminal and the base of said second transistor (Q12),

a first constant current source (34) is connected between said first power source terminal and a connection point of the base of said first transistor (Q10), said first

switching means (Q18), and the emitter of said third transistor (Q14), and a second constant current source (36) is connected between said second power source terminal and a connection point of the base of said second transistor (Q12), said second switching means (Q20) and the emitter of said fourth transistor (Q16), for permitting current to flow in a first direction from said first constant current source (34) to said first control terminal in the holding mode and preventing the flow of current in the first direction in the sampling mode, and for permitting current to flow in a second direction from said second control terminal to said second constant current source (36) in the holding mode and preventing the flow of current in the second direction in the sampling mode, and

the collectors of said second and third transistors (Q12, Q14) are connected to said second power source terminal, respectively."

VI. Essentially the Appellant submits the following arguments:

Document D1 does not show or even suggest any specific means for generating the current pulses for controlling the sample and hold circuit (S&H-circuit). In D1 a reference is made to D4. This document, however, discloses a pulse network that supplies constant currents to the S&H-circuit during the sample mode and back-biases the S&H-circuit during the hold mode. Thus the operation principle is quite different from the present invention. D3 relates to voltage-controlled diode quad gate circuits and the bridge and mode-switching principle in this case is completely different from the arrangements of D1/D4. Therefore, a skilled man would not combine this teaching with the one of D1/D4.

Reasons for the Decision

1. The appeal is admissible.

2. Valid Claim 1 is principally a combination of original Claim 1 and most of the features of original Claims 2 to 5 and can be read onto Figure 3 of the application and the corresponding text of the description. Claim 2 contains features taken from original Claim 3. Claim 3 contains features taken from original Claims 6 and 8 and Claim 4 corresponds to original Claim 7.

The requirements of Article 123(2) EPC are accordingly satisfied.

3. Claim 1 is delimited against D1 and its subject-matter is clearly novel with respect to any of the documents cited in the decision under appeal or in the European search report. The issue to be decided is whether it involves an inventive step.

3.1 Originally according to the description of the present application it was considered that the problem to be solved by the alleged invention was "to provide a sample and hold circuit (S&H-circuit) operable at high speed with high reliability".

At that time the starting point of the alleged invention was considered to be the S&H circuit according to Figure 1 of the application. This circuit shows principally a diode bridge (12) which has two nodes connected to two different constant current sources (18,20) and two nodes to the input and output, respectively. One of the constant current sources (18) is connected to a supply voltage (E1) and the other one (20) to ground. Moreover, this circuit has a driving control means including a pulse generator (22) and

a current control circuit (Q6,Q5) to set the sample and holding modes and to control the driving currents.

This circuit corresponds to the one of D3, since all the transistors shown in Figure 1 of the application are arranged to perform like normal diodes.

During the examination procedure, Claim 1 was delimited against D1 which is concerned with a S&H-circuit included in a derivative circuit. This circuit is designed in the form of a transistor bridge and is of the so-called diamond type. Thus the transistors must be controlled by gating pulses. However, in D1 it is not clearly disclosed in which way the controlling circuit is designed. The problem to be solved by the present invention can, therefore, be considered to be the one as originally stated in the description of the application, as a more specific and still objective problem cannot be found.

However, a skilled person is always concerned with such and similar improvements in order to increase the efficiency, to simplify the design or to decrease the costs of apparatuses, and the formulation of the technical problem at the basis of the present invention, therefore, lies within his normal activity.

3.2 The diamond circuit of D1 differs from the circuit defined in the prior art portion of Claim 1 in that the collectors of said second and third transistors are connected to a third power source terminal (minus terminal). The Board agrees, however, with the Examining Division that it would be obvious for a skilled person to change the said circuit in D1 - if the input signal always is of one polarity - in such a way that the collectors of transistors 18 and 20 are connected to ground instead of to a third terminal. Thus, the last characterising feature of Claim 1 is to be considered as obvious to a skilled person.

3.3 In the decision the Examining Division said that D1 itself did not show any specific means for generating current pulses used for controlling the S&H-circuit. Although in D1 reference was made to D4 in which a control circuit for a S&H circuit was shown, the Examining Division stated that the skilled man would not use that control circuit since it was not suitable for integration because of the presence of transformers. However, by studying the function of the circuit in D4 it would be obvious to a skilled man - having regard to the teaching of D3 - to introduce first and second constant current sources and a mode setting means in the circuit of D1 and so arrive at a S&H-circuit defined by Claim 1.

3.4 To the Board it appears that a skilled person when discovering the reference in D1 to the teaching in D4 would not so easily refrain from the teaching of D4 and thereafter try to adapt the teaching of D3 to the S&H-circuit in D1. It belongs to the normal consideration of a skilled person in this technical field to realise that the transformers in the circuit of D4 would not be appropriate for the desired application of the circuit in an integrated circuit. Therefore, he would attempt to avoid them by redesigning the disclosed control circuit or by using another circuit: in D4, page 22 it is already said that a number of methods exist for developing the pulsed gate currents required by a diamond. Furthermore the Examining Division in its decision feels - contrary to the Appellant - that the circuit in D4 in certain respects (decharging of parasitic capacitances) has just as good properties as the circuit according to Claim 1. Thus it appears that it would not at all be self-evident that the skilled person would abandon the prior art disclosed in D4 and turn to another teaching.

3.5 D3 discloses various switching arrangements for diode quad gates which are based on the prior art bridge referred to under 3.1 above. There appears to be no hint in this document to the possibility of using these arrangements for switching of circuits like the transistor diamond circuit disclosed in D1. This is understandable as D3 (Figure 1) discloses a gate circuit arrangement including a voltage source by which constant currents from constant current sources are by-passed in the hold mode, while during sampling those same currents are charging/discharging the capacitor through the associated diode bridge. The capacitor is thereby charged and discharged through the said constant current sources, whereas the capacitor in D1 is supplied by constant voltage sources via collector - emitter paths of transistors (20 and 24 in Figure 3 in D1), which are controlled by signals provided by pulsed constant current sources (e.g. as disclosed in D4 - cf. Figure 24, transistors Q1,Q3 act as constant current sources).

Thus, the constant current sources in D3 are in the main current path - thereby supplying the capacitor - and they must deliver relatively large currents (10 mA) in order to avoid a long charge/discharge time of the capacitor. On the contrary, the pulsed current sources in D4 produce only control signals for control electrodes (bases) of switching elements (transistors) in the bridge circuit proper.

D3 only discloses circuits comprising diode quad gates, i.e. bridge circuits, of which the arms comprise solely diodes and no independently controlled transistors. Since D3 does not show in any of the bridge arms transistors which are controlled by the same control circuit, it does

not teach how signal currents for the control electrodes of such transistors can be provided. Therefore, it does appear most unlikely that a skilled man in his normal work would turn to the teaching of D3, even if he would find that the teaching of D4 does not correspond to his expectations.

3.6 It is true that by replacing the bridge in Figure 1 in D3 by the diamond bridge disclosed in D1 and by connecting and adapting the corresponding terminals to each other as proposed by the Examining Division, a circuit according to Claim 1 would result. However, such a combination appears to be the result of an ex post facto analysis which is possible only after the solution has become known.

Thus, already the fact, mentioned above, that the teaching of D1 in combination with D4 leads the skilled man away from the circuit configuration proposed by present Claim 1 indicates that there is an inventive step.

Also it appears that the claimed S&H-circuit is operable at a high speed. In D4 the transistors Q1,Q3 are abruptly switched off and "pull-back" transistors Q2,Q4 are necessary to reverse the potentials of the nodes in order to ensure an improved pulse form. Thus, the design of the circuit for pulsing the constant current sources Q1,Q3 and the additional transistors Q2,Q4 in D1/D4 appears to be much more complicated than the one of the claimed circuit. It thereby appears that the creation of all the pulses necessary for activating the switching elements in the control circuit itself and in the bridge (e.g.appropriate transformer pulses for Q1,Q3 and thereafter for transistors Q2, Q4) must be very time consuming, and decrease the operating speed of the known circuit as a whole.

According to the application, the current is not abruptly switched off, the potentials of the nodes of the bridge are not reversed and a complicated control system is not necessary. Instead, during the holding phase, the currents from the unpulsed constant current sources 32,34 are smoothly drawn through the switching transistors Q18 and Q20 by the voltage generating circuit 40.

In its decision the Examining Division also appears to admit that the circuit according to the invention enables faster switching between modes, but concludes that this effect is not surprising, since switched current sources are known to have superior switching speed over e.g. the pulse circuit in D4. The Board admits that this effect when taken isolated is not surprising, but the question is whether the skilled person, when starting from D1, would have tried to apply it. It is clear that he could have done it, but as pointed out above, since D1/D4 teaches away from the claimed invention the Board is of the opinion that the skilled person would not have done it.

3.7 It is accordingly the Board's view that the subject-matter of Claim 1 is not obvious to a person skilled in the art having regard to the references cited. Thus, the required inventive step within the meaning of Article 56 is not lacking.

4. Claim 1 and dependent Claims 2 to 4 are, therefore, allowable having regard to Article 52(1) EPC.

Order

For this reason, it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a European patent on the basis of the documents cited under numeral IV of Summary of Facts and Submissions.

The Registrar: The Chairman:

M. Kiehl P.K.J. van den Berg