BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS | BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE | CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

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File Number: T 707/90 - 3.5.1

Application No.: 82 306 312.8

Publication No.: 0 080 875

Title of invention: Data storage system for a host computer

Classification: G11C9/06

D E C I S I O N
of 17 February 1992

Applicant: Storage Technology Corporation

Headword:

EPC Articles 56, 113(1)

Keyword: "Serious procedural error (no)"
"Inventive step (yes, after amendment)"

Headnote

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Case Number : T 707/90 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 17 February 1992

Appellant : Storage Technology Corporation
2270 South 88th Street
Louisville
Colorado 80027 (US)

Representative : D.S. Jackson
Reddie and Grose
16 Theobalds Road
London WC1X 8PI (GB)

Decision under appeal : **Decision of Examining Division 2.2.10.067 of the European Patent Office dated 8 May 1990 refusing European patent application No. 82 306 312.8 pursuant to Article 97(1) EPC.**

Composition of the Board :

Chairman : P.K.J. van den Berg
Members : A.S. Clelland
C. Holtz

Summary of Facts and Submissions

I. The Appellant contests the decision of the Examining Division refusing European Patent Application No. 82 306 312.8.

II. The reason given for the refusal was that the subject-matter of Claim 1 lacked an inventive step having regard to the prior art known from the following document:

D1: GB-A-2 052 118

III. On 4 July 1990 the Appellant filed a notice of appeal and subsequently paid the appeal fee. Cancellation of the decision in its entirety was requested. A statement setting out the Grounds of Appeal was subsequently filed on 24 August 1990.

IV. In a communication dated 27 February 1991 the Rapporteur referred, inter alia, to D1 and to the following document:

D3: Proceedings of the COMP-CON FALL-80 Conference, September 23-25 1980, Washington DC, USA, pages 412-41 TOKUNAGA et al: "Integrated disk cache system with file adaptive control"

V. The Appellant requests that the decision under appeal be set aside and a patent granted on the basis of the following documents:

Claims: Claims 1 to 4 as received on 5 February 1992

Description: Pages 1, 1a, 6 and 6a as received on 5 February 1992;
Pages 2-5 and 7 as received on 23 March 1989;
Pages 8-25 as originally filed, with the amendments to pages 12, 14 and 21 as proposed in the letter received on 8 August 1987

Drawings: Sheets 1-4 as originally filed

VI. Claim 1 reads as follows:

"A peripheral memory subsystem for use with a host computer (10) of the kind that incorporates an arithmetic and logic unit and a main memory unit for data and programs and is adapted to generate input/output commands directed to long-term data storage means through a plurality of memory access paths (16, 18), the peripheral memory subsystem incorporating access path control means (12, 24) including a first control unit (12) adapted to be connected to one (16) of the memory access paths, and a second control unit (24) connected to a long-term storage means (26), the subsystem further including solid-state cache memory means (30, 32) connected to the access path control means (12, 24) for holding data anticipated to be the subject of input/output commands and having a third control unit (32) adapted to monitor input/output commands at the access path control means (12, 24) and to provide instructions to the access path control means (12, 24) for the control of flow of data between a memory access path (16) to which the first control unit (12) is connected, the long-term storage means (26) to which the second control unit (24) is connected, and a memory unit (30) of the solid state cache memory means (30, 32), characterised in that the subsystem includes at least one further access path control

means (14, 24) including a first control unit (14) adapted to be connected to another one (18) of the memory access paths, and a second control unit (24) connected to another long-term storage means (26), that the solid-state cache memory means (30, 32) is also connected to the one further or each further access path control means (14, 24), that the third control unit (32) is adapted to monitor also input/output commands at the one further or each further access path control means (14, 24) and to provide instructions to the one further or each further access path control means (12, 24) for control of flow of data between the memory access path (18) to which the first control unit (14) of the particular further access path control means (14, 24) is connected in operation, the long-term storage means (26) to which the second control unit (24) of the particular further access path control means (14, 24) is connected, and the memory unit (30), and that the third control unit (32) examines data requested by the host computer (10) and determines whether sequentially stored data records stored in any of the long-term storage means (26) are likely to be subsequently requested by the host computer (10) and, if the determination is positive, controls transfer to the memory unit (30) of the data records anticipated to be the subject of such subsequent requests, the third control unit (32) so controlling the access path control means (12, 24; 14, 24) as to allow any first of a series of requests for a stored data record by the host computer (10) to be effected to the appropriate long-term storage means (26)".

Reasons for the Decision

1. The appeal is admissible.

2. Admissibility of Amendments

Claim 1 as originally filed was directed to a data storage system and included as characterising features first and second data paths, the first such path connecting the "secondary data storage means" (the long-term storage means) by way of the "control module" and the "director" (together the access path control means) to the cache memory. The second data path connected the cache memory through the "director" to the "channel" (and thence to the host computer).

None of these features are explicitly mentioned in Claim 1 as now presented, which is directed to a peripheral memory subsystem. The question accordingly arises as to whether the present Claim 1 is based on the disclosure of the application as filed. The claim refers to the access path control means controlling the flow of data between a memory access path (i.e. a channel), the long-term storage means and the cache memory; it also states that the cache memory is connected to the access path control means "for holding data anticipated to be the subject of input/output commands". These passages show that the access path control means provides data paths from the long term storage means to the cache memory and from the cache memory to the host computer. All the features of the original Claim 1 can thus be identified in the present claim, albeit in different terminology; the present claim is thus based on an appreciation of the invention derivable from the orginally filed application.

Claim 1 accordingly complies with Article 123(2) EPC and is admissible.

3. Procedural Violation - Article 113(1) EPC

In the grounds of appeal the Appellant in effect asserted that the Examining Division committed a substantial

procedural violation in rejecting the application, in that the second communication led the Appellant to believe that after specified amendment the application would be in order for grant.

A substantial procedural violation would arise if the application were rejected for a reason or on the basis of evidence on which the Appellant had not had the opportunity to present his comments, Article 113(1) EPC. The objection on which the application was rejected appeared in the first communication, in which inter alia D1 was cited. Reference was directed to Figures 6 and 10 of D1 and it was stated that:

> "...the "disk controller" (20) has the same structure as the "director" and the "control module" according to independent Claims 1 and 11 of the present application. Especially in the arrangement according to D1 the same data paths as stated in Claim 1 can be established... the sole structural difference between the subject-matters of Claim 1 and the independent claims consists in that, according to the present application, the main computer is a host computer. This difference, however, does not involve an inventive step..."

Revised claims filed in response to this and other objections were directed to a "peripheral memory subsystem" rather than the originally filed "data storage system" and the two-part formulation of Claim 1 was altered; otherwise the scope of the claim was maintained substantially unchanged. It was argued that the claimed invention was patentably distinguished from D1 since it provided an improvement which did not require any

modification to the host hardware or software. There is no doubt on the part of the Board that the response was bona fide.

In the second communication D1 was not mentioned explicitly but it was stated that

> "Your arguments regarding the differences between the prior art and the invention are noted. However, amended claim 1 does not clearly reflect these differences..."

Reference was then made to D3. There can be little doubt that the overall tone of this communication was such as to suggest that subject to clarifying amendment of Claim 1 and corresponding amendment of the description the application was in order for grant. Nevertheless, although the reference to D3 is confusing and possibly even a typographical error for D1, the above-quoted passage makes clear that because of the terminology used, the objection of lack of inventive step raised in the first communication was considered not to have been overcome.

The decision of the Examining Division was therefore based on grounds on which the appellant had had the opportunity to present his comments. The objection on which the application was refused was in substance raised in the first communication and, even if the second communication was somewhat obscure, no procedural violation falling within Article 113(1) EPC can be said to have taken place.

4. Novelty

4.1 In the Board's view the single most relevant document is D1.

4.2 Various figures of D1 refer to a "storage control unit" or "SCU" 18 which is in turn connected to a "disk controller" 20 for a number of disk drives. According to page 1, lines 10 to 13 the SCU "interprets the commands from the central processing unit and directs writing of information to or retrieval of information from disc devices". Connected to the disc controller 20 is a disc cache 16, described at page 4, lines 21 and 22 as "an intelligent, disc type specific, high speed memory interposed within the input/output subsystem architecture...", which in accordance with page 7 of D1 can operate in various modes to control the data flow between the CPU and the disc drives. D1 thus discloses a peripheral memory subsystem including access path control means in the form of a first control unit (SCU 18) and a second control unit (disc controller 20). From Figure 5 it can be seen that the disk cache includes a third control unit (cache control microprocessor 50) which provides instructions to the access path control means for the control of flow of data between the cache memory (54), the host (CPU 2) and the long term storage means (disc drives 14). The features of the preamble of Claim 1 can thus be found in D1.

4.3 None of the features of the characterising part of Claim 1 be identified in D1. The subject-matter of Claim 1 is accordingly novel.

5. Inventive step

5.1 The characterising part of Claim 1 is in essence directed to the following features:

(a) at least one further access path control means, a first control unit of which is connected to another

memory access path and a second control unit to another long-term storage means.

(b) The cache memory is connected to each access path control means, the third control unit controlling their operation.

(c) The third control unit determines whether sequentially stored records are likely to be requested by the host computer and if so transfers them to the cache.

5.2 In accordance with page 4, lines 37 to 44 of D1 the disc controller 20 is connected to a "string switch" 68, shown in Figure 6; it has not been disputed that this permits the controller 20 to be connected to a plurality of SCUs 18, i.e. that plural memory access paths are envisaged. Conversely, as indeed stated by the Appellant this implies that an SCU has access to a plurality of controllers. The skilled man would accordingly understand that a further access path control means including further first and second control units could be provided in D1.

5.3 As noted at paragraph 4.2 above, the D1 cache is said at page 4, line 21 to be "disc type specific", i.e. specific to the controller 20 and the string of drives 14 connected to it. Thus if the skilled man were to modify D1 to include a plurality of controllers as envisaged in paragraph 5.2 above the obvious manner of implementation would be to provide a separate cache for each controller rather than use only a single cache for all controllers as in the claim.

5.4 Moreover, the cache memory of D1 serves to store information in conformance with an algorithm based on most-recent-usage and least-recent-usage parameters, usage

referring to track usage, see page 5, lines 21 to 23 and page 9, lines 15 to 49. There seems no good reason why the skilled man should modify the D1 algorithm to determine whether sequentially stored records are likely to be subsequently requested; feature (c) calls for the monitoring of the data records by the third control unit of the cache and the storage of sequential records likely to be subsequently requested, rather than merely of track data.

5.5 The Board therefore considers that the subject-matter of Claim 1 involves an inventive step, having regard to the disclosure of D1.

5.6 The question of whether the skilled man would find it obvious to modify the D1 disclosure to take account of the teaching of D3 has also been addressed by the Board. D3 discloses at Figure 1 on page 413 a cache system in which a single disk cache is connected to a "system control unit". From page 414, "Sequential File mode" it can be seen that it is envisaged in D3 that in this mode files are "prefetched"; this appears to be the arrangement of feature (c) of Claim 1, see paragraph 5.1 above.

5.7 The D3 arrangement relies on a "system control unit" to which the I/O processor and the cache memory are directly connected for cache control. If the skilled man were to modify D1 to take account of the teaching of D3 he would be led to connect the cache memory to the CPU itself rather than in a peripheral subsystem.

6. For these reasons, in the Board's view, the subject-matter of Claim 1 involves an inventive step.

7. Claim 1 being allowable, the same applies mutatis mutandis to dependent Claims 2 to 4, which relate to specific embodiments of the peripheral memory subsystem of Claim 1.

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent on the basis of the Appellant's request (paragraph V. above).

The Registrar The Chairman

M. Kiehl P.K.J. van den Berg