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D E C I S I O N
of 5 January 1996

Case Number: T 0780/90 - 3.5.1

Application Number: 86201764.7

Publication Number: 0219907

IPC: H03K 3/037

Language of the proceedings: EN

Title of invention:
Integrated memory circuit

Applicant:
N.V. Philips' Gloeilampenfabrieken

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (denied)"

Decisions cited:
-

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0780/90 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 5 January 1996

Appellant: N.V. Philips' Gloeilampenfabrieken
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Decision under appeal: **Decision of the Examining Division of the European Patent Office dated 12 June 1990 refusing European patent application No. 86 201 764.7 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: P. K. J. van den Berg
Members: C. G. F. Biggio
E. M. C. Holtz

Summary of Facts and Submissions

I. European Patent Application No. 86 201 764.7, filed on 13 October 1986 and claiming the priority of patent application No. 8 502 811 filed in the Netherlands on 15 October 1985, was refused by a decision dated 12 June 1990.

II. This decision was based on the application as originally filed.

The Examining Division, having taken into account the following citations:

D1: PATENTS ABSTRACTS OF JAPAN, vol. 7, No. 84, 8 April 1983 & JP-A-58/10915;

D2: US-A-3 339 089;

D3: THE RADIO AND ELECTRONICS ENGINEER, July 1966, pages 33 to 45;

D4: EP-A-0 130 645, and

D5: EP-A-0 092 663,

considered that the subject matter of Claim 1 lacked an inventive step, pursuant to Article 56 EPC, over the teaching disclosed by D1 and D2.

III. On 7 August 1990 the Appellant filed an appeal against said decision. Grounds of Appeal were also filed at the same date.

The appeal fee was paid on 13 August 1990.

The Appellant's arguments can be summarized as follows:

The invention related to an integrated memory circuit controlled by a clock signal and a data signal and including a memory loop with a clock controlled first gate and a clock controlled second gate; the originality of said memory circuit was to be seen in that, in order to avoid the so-called "race condition", the switching threshold of the first gate deviated substantially from the switching threshold of the second gate.

In respect of the opposed citations D1 and D2, the Appellant made the following submissions.

D1 described a memory circuit which corresponds with the one shown in Figure 2 of the application, insofar as the arrangement of the logic gates constituting the memory circuit is concerned.

However, D1 was fully silent about the dynamical behaviour of the memory circuit it discloses.

D2 dealt with the problem of avoiding "race condition" in a latching circuit including a loop with two logic gates and receiving two complementary latch-signals and a data signal.

It was, however, pointed out that:

- the implementation of the circuit disclosed by D2, in bipolar technology, used the explicit presence of an emitter follower in the relevant logic gate in order to introduce a slight delay and, as a consequence, to avoid a "race condition", and

- this delay generated by the additional emitter follower shifted the switch-over point of the relevant logic gate in time, with respect to the external clock.

The Examining Division had mistaken the time-shifting, generated by the additional emitter follower according to D2, for the mutual shifting of switching thresholds of logic gates in the input-output characteristic of logic gates. The shifting along the time axis by means of the emitter follower, as proposed in D2, did not imply the presence of mutually different switching thresholds of the logic gates in the loop.

IV. In a first communication of the Board, dated 14 August 1990, an objection of lack of an inventive step, based on prior art documents D1, D2, D4 and D5, was raised in respect of Claim 1, as refused by the Examining Division.

V. In response to this communication, the Appellant filed - on 18 December 1991 - an amended Claim 1 which reads as follows:

"An integrated memory circuit, including a clock input for receiving a clock signal, a data input for receiving a data bit under the control of the clock signal, and a data output, the memory circuit also including a memory loop comprising a first and a second gate that both are switchable by the clock signal, **characterized** in that a switching threshold of the first gate deviates substantially from a switching threshold of the second gate".

The Appellant requested that the appealed decision be set aside and a patent be granted on the basis of the above quoted Claim 1.

VI. In a second communication of the Board, dated 10 September 1992, reference was made to the complete specification of D1 and to an available translation thereof.

After a detailed analysis of D1, the Board

- stated that, in respect of the disclosure of said citation, the novelty of the subject-matter disclosed by the pending application should be considered as merely restricted to the following feature: "**the switching threshold of the first gate (1 or 11) deviates substantially from the switching threshold of the gate combination (6 or 16)**", and

- expressed its negative opinion on the patentability, pursuant to Articles 52(1) and 56 EPC, of the subject-matter of said claim, having made further reference to

- citations D5 and D4, and

- general common knowledge of a person skilled in the art.

VII. In his reply to the second communication, filed on 15 January 1993, the Appellant did not dispute the Board's conclusions, with regard to the novelty of the subject-matter claimed by Claim 1.

However, on the issue of inventive step, the Appellant argued as follows:

- D5 did not specify that "race condition" may be avoided by making the switching threshold of the first gate deviating substantially from the switching threshold of the second gate.

- The gate delay based technical approach of D4 lead away from the invention, because the summing of individual gate transit time is not applicable to the circuit according to the application.

- The Board's negative opinion, based on common general knowledge of a person skilled in the art, was not substantiated by reference to any standard book.

- The subject-matter of Claim 1, as filed on 18 December 1991, was therefore novel and inventive over any cited prior art, and could not be rendered obvious by common general knowledge of a person skilled in the art.

The Appellant subsidiarily requested that oral proceedings be appointed, if the Board should envisage to dismiss the Appeal.

VIII. On 15 December 1993, the Board informed the Appellant of its intention to schedule the requested oral proceedings for 11 February 1994.

IX. On 21 December 1993, the Appellant withdrew his request for oral proceedings, made further reference to his submissions, as filed on 15 January 1993, and maintained his request that the appealed decision be set aside and a patent be granted on the basis of Claim 1, as filed on 18 December 1991.

Reasons for the Decision

1. *Formal questions*

1.1 The appeal complies with Articles 106 to 108 and Rule 64 EPC and is therefore admissible.

1.2 Although in the communication dated 10 September 1992 it was indicated that an objection under Article 84 EPC seemed to arise, the Board will not discuss this issue, since the appeal must fail on other grounds as will be indicated below.

2. *Novelty*

As the analysis on novelty - stated in the communication of 10 September 1992 - is not in dispute, it suffices here to repeat the Board's conclusions that D1 discloses an integrated memory circuit showing all the features mentioned by the precharacterising clause of Claim 1, so that the novelty of the subject-matter claimed has to be considered as restricted to the following feature: "**the switching threshold of the first gate (1 or 11) deviates substantially from the switching threshold of the gate combination (6 or 16)**".

3. *Inventive step*

3.1 The Board notes that, according to the pending application (column 2, line 25 to column 3, line 28), the novel technical feature mentioned in Claim 1 and represented by the switching threshold of the first gate (1, 11) deviating substantially from the switching threshold of the gate combination (6, 16) is intended to

ensure that the memory circuits claimed fulfil the following dynamical conditions of functioning, under which "race condition" may be avoided:

(a) the first gate (1) must react comparatively more quickly to the clock signal transition from "low" to "high" than the gate combination (6) (column 2, line 51 to column 3, line 3), respectively, b) the first gate (11) must react comparatively more quickly to the clock signal transition from "high" to "low" than the gate combination (16) (column 3, lines 21 to 28).

3.2 D5 discloses a polarity hold latch comprising two latched gates, which receive simultaneous control clock inputs, and a data input gate, in which the first one of said two latched gates is relatively faster than the second one (see Claim 1) and in which neither circuit is deliberately slowed down by the addition of any extraneous component introduced for this purpose (see page 2, lines 10 to 12).

Thus, D5 discloses, explicitly and almost in the same words as the present application, the dynamical conditions of functioning, under which "race condition" may be avoided.

The fact that citation D5 does not specify that "race condition" may be avoided by making the switching threshold of the first gate deviating substantially from the switching threshold of the second gate and is therefore not regarded by the Board as a sufficient ground to consider its teaching as irrelevant.

3.3 D4 discloses an integrated divider-by-two-circuit of the master-slave kind (see e.g. Claim 1), which is controlled by only one clock signal. Said citation

deals, inter alia, with the problem of avoiding oscillations which may arise in such a circuit on account of "race condition" and proposes a plurality of possible solutions of said problem (see page 7, lines 6 to 21).

Among said plurality of possible solutions, D4 mentions explicitly (page 7, line 19 to 21) that of mutually shifting the switching threshold of the gates comprised in the master, thereby obtaining the suitable slow down of said gates and fully overcoming the problem of oscillations which may arise from "race condition".

Thus, D4 discloses, in the context of the master-slave flip-flop circuits which are also envisaged by the present application (column 4, line 54 to column 5, line 3; Claims 8 and 9), a similar solution summed up by the feature: "**the switching threshold of the first gate (1, 11) deviates substantially from the switching threshold of the gate combination (6, 16)**".

In the Boards's opinion, the Appellant's submission against the pertinence of citation D4, i.e. "contrary to the invention, the gate delay, based on the technical approach according to D4, is dependent on the delays of the individual gates", is not correct, since the pending application (column 1, lines 28 to 38) merely states that, in memory circuits of the kind referred to, the correct storage of a data bit may be dependent on the signal propagation through the individual gates, but does not disclose any specific feature intended to render the gate delay independent from the delays of the individual gates.

On the contrary, in the pending application (column 2, line 51 to column 3, line 1) it is stated that "race condition" is avoided by ensuring that the output (QB)

of the gate combination (6) reacts comparatively slowly to the transition from "low" to "high" of the clock signal applied to its input, while the first gate (1) must show the opposite dynamical behaviour.

In the Board's opinion, accordingly, the disclosure of the pending application referred to hereabove implies

- that the transit time of the gate combination (6), **which is made up by the sum of the individual transit times of gates (3) and (2)**, must be longer than the transit time of gate (1) alone, and consequently,

- that the gate delay, based on the technical approach according to the pending application, **is not independent of the delays of the individual gates**, as alleged by the Appellant.

3.4 Moreover, any person skilled in electronics is well aware that, in the physical reality, a square wave -like a clock signal-

- is never such that it may be considered as a periodical repetition of the Heaviside's "Unit Step Function", but, on the contrary,

- is always such that it shall be considered as the periodical repetition of a "trapezoidally" shaped pulse, since its amplitude needs a given amount of time to pass from "low" to "high", respectively from "high" to "low".

Any person skilled in electronics is hence well aware that, if such a periodical repetition of a "trapezoidally" shaped pulse is simultaneously applied to the respective inputs of two gates having different

switching thresholds, the respective outputs of said gates will follow their respective inputs in the following manner:

(a) for a transition from "**low**" to "**high**" of the input signal, the output of the gate having a lower switching threshold will follow its input **sooner**, in time, than the output of the gate having a higher switching threshold, while,

(b) for a transition from "**high**" to "**low**" of the input signal, the output of the gate having a higher switching threshold will follow its input **sooner**, in time, than the output of the gate having a **lower** switching threshold.

The above-mentioned considerations and conclusions do not need to be substantiated by a reference to any standard textbook, since they form part of the basic knowledge of a fresh graduate in electronics.

3.5 Following the considerations mentioned in previous points 3.1 to 3.4, a person skilled in electronics, faced with the problem of avoiding "race condition" between two gates - said problem being not mentioned explicitly in D1 -, would have found that said problem was known to occcur in circuits of the type disclosed by D1, and solved both by D5 and D4.

He would have been taught, by D5, to solve said problem by making the first one of said gates to react comparatively more quickly to a clock signal transition than the second one of said gates (see previous points 3.1 and 3.2).

He would have been taught, by D4, that the above behaviour of the two gates could be obtained, inter alia, by making the switching threshold of one gate substantially higher (or conversely lower) than the switching threshold of the other gate (see previous point 3.3, second and third sentences thereof).

He would, moreover, have been encouraged to choose the above mentioned solution, among the various proposed by D4, by his fundamental background knowledges in electronics (see previous point 3.4).

He would hence immediately have envisaged that, in an integrated memory circuit showing the same structure as that disclosed by D1, he might solve the problem of avoiding "race condition" between two gates by acting on the respective switching thresholds of said two gates, namely by making the switching threshold of one gate substantially higher (or conversely lower) than the switching threshold of the other gate, which sums up to the same kind of solution which is claimed by the novel feature mentioned in the characterising clause of Claim 1.

3.6 The Board is, accordingly, of the opinion that the subject-matter of Claim 1 does not involve an inventive step as required by Article 52(1) and as specified by Article 56 EPC.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

M. Kiehl P. K. J. van den Berg