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BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE

CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

Publication in the Official Journal ~~Yes~~ / No

A		B		C	X

File Number: T 43/91 - 3.5.1

Application No.: 85 105 715.8

Publication No.: 0 161 639

Title of invention: Self-contained array timing

Classification: G11C 29/00

D E C I S I O N
of 31 July 1992

Applicant: International Business Machines Corporation

Headword:

EPC Article 56

Keyword: "Inventive step (yes, after amendment) - unobvious modification of obvious implementation of known device"

Headnote

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number : T 43/91 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 31 July 1992

Appellant : International Business Machines Corporation
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Decision under appeal : Decision of Examining Division 067 of the European Patent Office dated 10 September 1990 refusing European patent application No. 85 105 715.8 pursuant to Article 97(1) EPC.

Composition of the Board :

Chairman : P.K.J. van den Berg
Members : W.B. Oettinger
W.M. Schar

Summary of Facts and Submissions

I. The appeal contests the decision, dated 10 September 1990, of the Examining Division to refuse the European patent application No. 85 105 715.8 which, claiming a priority of 18 May 1984, was filed on 10 May 1985 (publication No. 0 161 639).

The reason given for the refusal was that the subject-matter of apparatus Claim 1 filed on 6 July 1990 did not involve an inventive step against the prior art known from

D1: JP-A-58-159 293,

particular reference being made to its abstract in

D1a: Patent Abstracts of Japan, vol. 7, no. 86, (P-244)[1431], 21 December 1983.

The same conclusion was drawn for the dependent claims and for the independent method Claims 6 and 7 filed on 7 August 1990.

II. The appeal was lodged, and the respective fee paid, on 30 October 1990 with a request that the decision under appeal be cancelled and a patent granted.

On 7 January 1991, the Appellant filed a Statement of Grounds accompanied by and referring, inter alia, to

D1t: an English translation of the text of D1.

III. In a Communication pursuant to Article 11(2) Rules of Procedure, the Board expressed its doubts whether the subject-matter claimed could be regarded as non-obvious.

In respect of the recirculating loop for testing claimed in one of the dependent claims, the Board cited

D2: JP-A-58-201 149,

referring in particular to its abstract in

D2a: Patent Abstracts of Japan, vol. 8, no. 51, (P-259)[1488], 8 March 1984.

IV. In response, the Appellant filed amended claims to be considered as auxiliary requests.

V. In oral proceedings held on 2 April 1992, the Appellant upheld his first auxiliary request of 3 March 1992 with the proviso that in the characterising part of Claim 1 the word "recirculating" is introduced before "tapped delay line" and the words "with means for initiating a test mode of the delay line" are introduced after "tapped delay line".

V. In support of this request he submitted, in essence, that no hint is given in either D1 or D2 to test a memory array chip by testing its timing control network made up of a tapped delay line made recirculating in the test mode.

VI. At the conclusion of the oral proceedings, the Board gave the Appellant a time limit to amend the description in order to adapt it to the claims and to acknowledge the prior art (D1, D2) and to file a fair copy of the claims.

VII. On 22 May and 21 July 1992, the Appellant filed amended application documents and requested that a patent be granted on the basis of documents which are understood to comprise the following:

- description: pages 1, 3 to 6 and 6a filed on 21 July 1992,
  page 2 filed on 6 July 1992,
  pages 2a, 2b and 12 filed on 22 May 1992,
  pages 7 to 11 as published;

- claims: 1 to 7 filed on 22 May 1992;

- drawings: sheets 1 to 6 as published.

The independent claims read as follows:

"1. An integrated circuit chip, containing a memory array (12), said memory array including:

a plurality of memory elements for storing binary data, said stored binary data being arranged within said array at a plurality of addressable locations;

controllable write circuit means for writing data into storage at a predetermined address within said array;

controllable read circuit means for reading data stored at a predetermined address within said array;

gated address latch circuit means (21) coupled to said controllable write circuit means and said controllable read circuit means, said gated address latch circuit means (21) providing said predetermined address to said write circuit means or said read circuit means;

gated data input latch circuit means (20) coupled to said controllable write circuit means, said gated input latch circuit means providing data to be written into storage at said predetermined address provided by said gated address latch circuit means (21);

gated data output latch circuit means (22) coupled to said controllable read circuit means, said gated output latch circuit means receiving the binary data read from the predetermined address by said controllable read circuit means; and

timing control network means (19) coupled to and controlling said controllable write circuit means and said controllable read circuit means, said timing control network also being coupled to said gated address latch circuit means, said gated data input latch circuit means and said gated data output latch circuit means, said timing control network on said integrated circuit chip providing all timing control signals (45-48) for the operation of said memory array contained on said integrated circuit chip upon receipt of a trigger signal (16);

characterised in that said timing control network (19) includes a trigger signal responsive recirculating tapped delay line with means for initiating a test mode for said delay line and a test output terminal (44) for providing a test signal."

"6. Method for testing the timing control network (19) of the integrated circuit chip according to any of the above claims comprising the following steps:

(a) triggering said timing control network (19);

(b) recording the signal produced at said test output means (32, 44);

(c) measuring the frequency of oscillation of said produced signal using a counter and time source."

Reasons for the Decision

1. The appeal is admissible (Articles 106 to 108 and Rule 64 EPC).

2. Amendments

No objection under Article 123(2) EPC arises against the amendments made.

2.1 The preamble of Claim 1 corresponds to the whole of Claim 5 as originally filed.

The characterising feature of the inclusion of a trigger signal responsive tapped delay line is based on the original Claim 8; the features of the original Claims 6 and 7 to which Claim 8 referred are considered still to be implicit in Claim 1 on file.

The further characterising feature, that the delay line is recirculating, is taken from the original Claim 12, in particular from the feature relating to "a second AND-INVERTER circuit (31)" (page 18, lines 14-18). It is considered that there is no necessity of restricting Claim 1 further to the entirety of all features listed in that Claim 12.

The further feature that there are means for initiating a test mode, is taken from the same feature of the original Claim 12 in connection with its feature relating to "a control input terminal (43)" (page 17, lines 19-20) and, as to the function of said "control", with the description relating to the test mode (page 11, lines 25 ff).

Finally, the feature that there is a test signal output means, is taken from the original Claim 13 interpreted as referring to Claim 12 (not "14"). It is considered that it is not necessary to restrict Claim 1 further to include also the remaining feature of that Claim 13.

2.2 The dependent device claims are based either (2) on the original Claim 9, or (3) on one of the features of original Claim 12, or (4) on the rest of that Claim 12, or (5) on the remaining feature of the original Claim 13.

2.3 The independent method Claim 6 is based on the description of the test mode (page 11, lines 25-33).

2.4 The same applies to dependent method Claim 7 (page 11, line 33 to page 12, line 1).

2.5 The amendments made to the description do not introduce any undisclosed matter either.

3. Clarity, claim partitioning and novelty

3.1 For the claimed integrated circuit chip with a memory array, the best prior art starting point on file is still represented by D1 and D1a.

3.2 From D1(a), all features listed in the precharacterising portion of Claim 1 (cf. paragraph VII) are known.

With particular reference to the timing control network means (19) featuring in the preamble, this feature is anticipated by the clock generator 43 in the internal control timing generator circuit 41 (cf. D1t) of the memory device shown in Figure 4 of D1.

The controllable (write, read) circuit means (within 12) and gated (address, data input, data output) latch circuit means (20-22) controlled by that timing control network (19) correspond to, or are associated with, the (row, column) decoders (57, 56) and (address, data in, data out) buffers (47, 58, 59) of D1(a), it being not relevant for the present case whether or not such further gating means as are shown within block 41 of D1(a) are incorporated either within the controllable write and read circuit means of the memory array (12) or within the gated address, data input and data output latch circuit means (20-22) or within the timing control network means (19) of the claimed i.c. chip.

3.3 In the characterising portion of Claim 1 (cf. paragraph VII), the following additional features can be identified:

(a) the timing control network (19) is a tapped delay line, which is, in the context of the present case relating to digital circuitry, to be interpreted as a tapped chain of delay elements connected in series (that this delay line is "trigger signal responsive" is a mere repetition from the last statement in the preamble and can, as such, be disregarded in the present analysis);

(b) there are means initiating a test mode for testing the delay line;

(c) the delay line is recirculating and has a test signal output terminal (44).

It is noted, at this instant, that the "recirculating" feature should, as a matter of course, not be mis-interpreted as a steady state feature of the tapped delay

line during "normal" operation of the memory array chip, it appearing self-evident that recirculation would be prejudicial to, and therefore undesirable in, normal write and read modes. Therefore, the above analysis takes into account that, correctly interpreted, Claim 1 is, and should be, understood as meaning that the delay line (feature a) is made recirculating (feature c) by the means initiating the test mode (feature b) (these means including gate 31 controlled by test control signal 43).

3.4 Feature (a) is clearly new against D1a and D1 (taking D1t into account). D1a does not show how the clock generator (43) should (internally) be implemented; and from D1t no further information is derivable apart from the fact that the output terminals 1 to 6 are intended to deliver differently delayed signals.

Features (b) and (c) are also clearly new against D1(a,t).

3.5 Therefore (3.1 and 3.4), Claim 1 is correctly partitioned (Rule 29(1)(a) and (b) EPC).

3.6 For the same reasons (3.1 and 3.4), the subject-matter of Claim 1 is clearly new (Article 54 EPC).

3.7 Claim 6 is an independent claim in respect of its category, i.e. its possible scope of protection.

But, by its reference to "the" network of "the" chip "according to any of the above claims", it fully incorporates all features of, at least, Claim 1 as if it were a dependent claim (Rule 29(4) EPC).

Furthermore, the claimed method steps are restricted to triggering "said" network (defined in Claim 1), recording

the signal at "said" output means (also defined in Claim 1) and measuring the frequency of "said" signal (recorded at "said" output means). It is therefore clear that Claim 6 must be construed as giving protection only for a testing method if and when the tested network is the particular network defined in Claim 1. (The word "for" is, in this particular case, not to be interpreted as meaning that the claimed method is only "suitable" for, but not limited to, testing the network of Claim 1.)

Therefore, no problem of clarity in respect of the wording of Claim 6 is seen (Article 84).

3.8 Claim 6 not being in the "characterised" two-part form, any problem of partitioning cannot arise (Rule 29(1)).

3.9 For the aforementioned reason (3.7 in combination with 3.6), the claimed method is to be regarded as new, irrespective of whether its steps are, or are not, known in a more general, or a different, context (Article 54).

3.10 No problem of any such kind, e.g. lack of clarity, arises with the dependent device or method claims.

4. Inventive step

The issue remaining to be decided is lack of inventive step (Article 56 EPC)

4.1 In D1a it is not shown, and in D1t no further information is given, how the clock generator (43) of D1 should be implemented.

The Examining Division has assumed, from its own knowledge, that, for deriving a series of differently timed pulses from a trigger pulse, a tapped delay line,

i.e. a tapped serial chain of delay elements, is common general knowledge. The Appellant has never really disputed this assumption. The Board, without having to resort to any respective prior art document, is of the same opinion. Thus, it would seem that it was correct to refuse the application on the basis of a claim which contained, in its characterising portion, only the said feature (a).

However, Claim 1 now containing further features, this is not the issue to be decided.

4.2 In D1, taking account of D1t, and in D1a no hint as to possible means allowing a test is found.

However, testing of integrated circuits of all kinds, particularly those including memory arrays and their control circuitry, is clearly a commonplace necessity (confirmed by the cross-reference and background prior art part of the application). Providing means for initiating a test mode cannot therefore be considered as unobvious.

But no incentive can be derived from D1 (D1t) or D1a to test specifically the delay line assumed to implement the clock generator (43). From general considerations of the skilled person it would appear more urgent to test the memory array (itself).

In contrast, according to feature (b), in the claimed invention the delay line is tested in the test mode. Apparently, this feature is based on the recognition that this can very easily be done, that it can be done on-chip without any access problems, and that with some certainty it can be concluded from the result of this test that the chip is defective possibly also in the nearby region of the memory array itself. Such recognition cannot be derived from D1.

Feature (b) is therefore considered not to be obvious from D1 (D1t) and/or D1a, having regard also to general knowledge.

4.3 The considerations (4.2) made in respect of means for initiating a test mode, apply similarly to test signal output means:

Providing such means, in a general case, on an i.c. chip would appear obvious but providing specifically the tapped delay line, assumed to implement the clock generator (43) of D1(a), with such a terminal, cannot be considered to be obvious from D1(a,t), even when general knowledge is taken into account.

Furthermore, even when it is assumed that it is obvious to implement the clock generator (43) of D1(a) as a tapped delay line, no hint can be found in D1 (D1t) or D1a to add to this delay line a feed-back path creating thus a recirculating loop.

Feature (c) is therefore not obvious from D1 (D1t) or D1a, even when account is taken of general knowledge.

4.4 From D2, an integrated circuit is known which contains an "internal logical element" (1), whose internal function is not further specified in D2a, and a number of output buffers (2) operatively connected in parallel to a corresponding number of output terminals of the internal logical element.

To detect a fault of an output buffer, or for testing the delay "timer" (sic; interpreted as "time") of the output buffer (or rather: buffers), D2a proposes to disconnect, by means of a corresponding number of selecting circuits

(4) controlled in a test mode from a test terminal (5), the buffers from the internal logical element (1), to connect them, by the same selecting circuits (4), in series and to connect the output of the highest-order stage (via amplifier 6) to the input of the lowest-order stage. By this arrangement, if self-oscillation is not performed this is an indication for a fault in the buffers, and if self-oscillation is performed, its frequency is a measure of the buffer delay time, whereby any of the normal output terminals (3) can serve as the test signal output terminal. The arrangement is said to be "used suitably for testing an integrated circuit".

It is noted, however, that the group of output buffers (2) of D2a does not a priori constitute a delay line. Rather, it is a parallel arrangement connected to parallel output terminals of the internal logical element (1). It is apparently their normal function to effectively isolate the downstream stages (connected to outputs 3) from the internal logical element (1) in the reverse signal flow direction and, possibly, to amplify the output signals. But their delay time is only a technologically inevitable, otherwise undesired, feature of these buffers. It can therefore be assumed that the designer of the integrated circuit of D2a would minimise these delay times and testing them is intended to check whether their minimisation was successful. The fact, that in the test mode, and only then, the output buffers are connected serially to effectively form a delay line, does not therefore mean that D2a teaches to test a delay line.

4.5 Thus, it would only appear obvious to use the arrangement of D2a for testing an i.c. chip, for instance one containing a memory array, if this chip has a parallel arrangement of output buffers as shown in D2a.

No incentive can be derived from this or any other statement in D2a to test specifically a clock generator, as that (43) of D1(a), designed to deliver differently delayed output clocks.

Even after the presumably obvious feature (a) has been applied, i.e. the clock generator has been implemented as a tapped delay line whose elements are dimensioned to delay the trigger signal by well-defined multiple clock periods, would it not follow from D2a to test this delay line. Given (cf. paragraph 4.4) that D2a teaches to test whether the undesired delay times, which the output buffer amplifiers of D2a inevitably have, are small enough not to impair the normal function of this circuit in the environment of a particular application, it would not be conclusive to derive therefrom a teaching to test a real delay line having the function of providing a series of output pulses intentionally delayed by different amounts.

Feature (b) cannot therefore be regarded as being rendered obvious by D2(a).

4.6 For this finding (4.5), it is not relevant that the implementation of the test is, in the claimed invention, ultimately similar to the implementation of the buffer delay check in D2a.

Only after the non-obvious decision has been made, in accordance with feature (b), to test the clock generator (43) of D1(a), assumed to be constituted by a tapped delay line, might it appear obvious to recognise that this test could be implemented by adding a test-mode controlled feed-back path to the delay line, and by providing specifically this recirculating delay line with a test signal output terminal. But such a finding of obviousness disregarding a preceding non-obvious step would be a

matter of hindsight and therefore an indamissible argument.

Feature (c) is therefore regarded, in the context of feature (b), as not being rendered obvious by D2(a).

4.7 Starting from the i.c. chip of D1 (D1t) and D1a, the claimed chip is therefore regarded as involving an inventive step, even having regard to the general knowledge and to D2(a).

Claim 1 appears, for these reasons, allowable.

4.8 The same conclusion is then to be drawn for Claim 6.

This claim is restricted, although in the independent method category, to a method of testing the particular timing control network of the i.c. chip claimed in Claim 1 (cf. 3.7) and found to involve an inventive step (4.7). The particular method of testing this network involves an inventive step on the same basis as a dependent claim derives its inventiveness from the independent claim to which it refers. It is unobvious to test the timing control network (19) by applying features (a), (b) and (c) of Claim 6 to the trigger signal responsive recirculating tapped delay line (cf. characterising portion of Claim 1, in particular feature (c) as defined in paragraph 3.3) for the very same reason as it is unobvious to render the timing control network (19) testable by making its delay line recirculating at all (cf. 4.3 and 4.6).

For a positive decision in the present case it is not, therefore, necessary to investigate whether the claimed method steps as such are novel in the field of testing generally. Nor is it relevant for this case that measuring the frequency of oscillation of the signal produced at a

test output of the recirculating delay line (cf. feature (c) of Claim 6) corresponds in fact to what is being done according to D2(a) for testing the integrated circuit known from that citation.

4.9 The dependent claims, defining particular embodiments, derive their allowability from their respective superior claim.

5. Other matters

No objection arises in respect of the description (Rule 27 EPC).

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent on the basis of the application documents on file (cf. paragraph VII).

The Registrar: The Chairman:

M. Beer P.K.J. van den Berg