BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS

BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE

CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

Publication in the Official Journal ~~Yes~~ / No

File Number: T 62/91 - 3.5.1

Application No.: 84 306 928.7

Publication No.: 0 142 266

Title of invention: Memory array

Classification: G11C 19/00

D E C I S I O N
of 17 June 1992

Applicant: Advanced Micro Devices, Inc.

Headword:

EPC Article 56

Keyword: "Inventive step (yes)"

Headnote

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number : T 62/91 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 17 June 1992

Appellant : Advanced Micro Devices, Inc.
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Decision under appeal : Decision of the Examining Division of the European Patent Office dated 3 September 1990 refusing European patent application No. 84 306 928.7 pursuant to Article 97(1) EPC.

Composition of the Board :

Chairman : P.K.J. van den Berg
Members : A.S. Clelland
E.M.C. Holtz

Summary of Facts and Submissions

I. European patent application No. 84 306 928.7 (publication No. 0 142 266) was refused by decision of the Examining Division dated 3 September 1990.

II. The reason for the refusal was that the subject-matter of Claims 1 to 8 as filed on 26 July 1990 with a submission dated 19 July 1990 lacked an inventive step having regard to the disclosure of the following documents (using the Examining Division's notation):

D1: US-A-4 151 609
D2: US-A-3 764 825.

III. On 2 November 1990 the Applicant lodged an appeal against this decision and paid the prescribed appeal fee. He appealed the decision in its entirety. On 8 January 1991 a Statement setting out the Grounds of Appeal was filed.

IV. In a communication dated 28 March 1991 the preliminary view was expressed that Claim 1 was not clear and that having regard to the disclosure of D1 the subject-matter of Claim 1 lacked an inventive step. In subsequent communications dated 21 June 1991 and 16 December 1991 further issues of clarity were raised; in the former communication the prior art document D2 was also discussed.

V. The Appellant requests grant of a patent on the basis of the following documents:

Claims: 1 to 8 filed on 10 February 1992.

Description: pages 1, 4 and 6 as originally filed; page 2 filed on 22 August 1991;

pages 3, 5 and 7 to 11 filed on 10 February 1992.

Drawings: sheet 1/2 filed on 10 February 1992; sheet 2/2 as originally filed.

VI. Claim 1 reads as follows:

"A memory array comprising a plurality of rows and columns of memory cells wherein each of the memory cells (0,0-4,31) has:

a first and second transistor (Q1,Q2) each comprising a plurality of electrodes including a first emitter (203,213) and a second emitter (205,215), a base (202,212) and a collector (201,211);

means (101,102) for coupling the second emitter (205,215) and the collector (201,211) of corresponding first and second transistors in adjacent rows; and

means for applying a predetermined control potential to the first emitters of the transistors for transferring a data bit of information between the first and second transistors and the corresponding transistors in an adjacent row,

characterised in that each of the first and second transistors (Q1,Q2) includes third emitter (204,214) and in that the means for applying the predetermined control potential is arranged to change the potentials on the first and third emitters from low to high potentials to selectively transfer data between the first and the second transistors and the corresponding transistors in the adjacent row."

VII. Claims 2 to 8 are either directly or indirectly appendant to Claim 1 and relate to further developments of the memory array of Claim 1.

VIII. In the Statement of Grounds of Appeal and in the submissions in response to the communications referred to at paragraph IV above, the Appellant argued that the subject-matter of Claim 1 was novel and inventive with respect to both D1 and D2. In particular, he argued that Claim 1 as now presented required the provision of memory cells comprising first and second transistors each having three emitters and means for applying a predetermined control potential to the first and third emitters so as to transfer data between the first and second transistors and between the corresponding transistors in the adjacent row of the array. In D1 only two emitters were present on each transistor and only a single, low, control potential was applied in order to enable a transfer; this had the disadvantage that if the low potential for transfer fluctuated, either no transfer would occur or uncontrollable transfer beyond the adjacent row could take place. By on the other hand providing two separate control potentials for respective emitters and requiring these to go high to achieve transfer this problem was overcome. D1 nowhere suggested the provision of a third emitter for the transistors and a skilled man would not be led by application of his common general knowledge to add such an emitter. Nor would he be led by the disclosure of D2 to arrive at the invention; D2 was explicitly concerned with the pre-setting of a serial shift register using a device with latent image capability; although D2 discussed the possibility of reading the content of each memory cell using the collectors of the transistors of the cell, D2 did not suggest the provision of a write operation using the collectors.

Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is, therefore, admissible.

2. The single independent claim, Claim 1, includes all the features of the broadest original independent claim, Claim 5. Neither Claim 1 nor any of the remaining amended application documents appear to the Board to contravene Article 123(2) EPC and are, therefore, admissible.

3. Clarity

3.1 In the correspondence with the Rapporteur clarity has been discussed extensively. In the Board's opinion the present Claim 1 does not give rise to objection under Article 84 EPC; though the claim makes use of the relative terms "high" and "low" in respect of the control potential applied in order to effect the transfer of data, the skilled man would - in the context of a memory array of the claimed kind - understand that the terminology relates to specific logic levels and would have no difficulty in interpreting the scope of the claim.

3.2 It is however noted that the application still includes a number of and clerical and other errors having no substantial significance. Since for the reasons given below the decision under appeal is set aside and the case remitted to the first instance, these errors are noted as follows:

Description

page 2, line 36:	delete "node 90"
page 3, line 28:	insert "a" after "includes"
page 4, line 3:	replace "second" by "third"
page 4, lines 6 and 8:	replace "third" by "second"
page 9, line 23:	replace "changes" by "change"
page 9, line 28:	delete "of"
page 9, line 29:	replace "a" by "as"

Claims

Claim 1, line 21:	insert "a" after "includes"
Claim 6, lines 2 to 5:	delete "wherein the means ... the third emitters (204,214)"
Claim 6, lines 8 and 9:	delete "the coupling means ... for coupling"
Claim 6, line 10:	insert "is coupled" after "transistors".

4. Novelty

4.1 The Board agree with the Appellant that the single most relevant prior art document is D1. The memory array known from D1 can be seen from Figures 1A and 1B to comprise a plurality of rows and columns of memory cells 10; from Figure 2B these memory cells can be seen each to comprise first and second transistors 480,482 each comprising a plurality of electrodes including a first emitter B, a second emitter A, a base 503,505 and a collector 504,506. Diodes 484,486 couple the second emitter and the collector of corresponding transistors in adjacent rows. A word line 90 applies a predetermined control potential to the first emitters B of the transistors for transferring a data bit of information between the first and second transistors and the corresponding transistors in an adjacent row.

4.2 D1 does not disclose the provision of third emitters for the memory cell transistors; the subject-matter of Claim 1 is accordingly novel.

5. Problem and solution

5.1 In accordance with the D1 arrangement, see column 7, lines 39 to 63, data is transferred between cells by causing the word line 90 of a row of cells to go low to

approximately 0.8 volts; if, in the arrangements shown in Figure 2B, transistor 482 is conducting and transistor 480 off, and if the word line of the adjacent row is high, then the effect of word line 90 going low will be to cause diode 486 to conduct thus causing the second emitter of transistor 513 of the adjacent row to be pulled low so that the transistor is turned on. In other words, data has been transferred from the cell of one row to that of the next row.

5.2 This known arrangement is discussed in the originally filed application. The known arrangement gives rise to the problem that because a low-going pulse is used to transfer the contents of one memory cell to another it is difficult to ensure reliable operation over a wide range of temperature and power supply voltages. Temperature and power supply fluctuations can result in the pulse not going low enough so that no transfer occurs, or alternatively going too low so that the contents of adjacent memory cells are uncontrollably transferred beyond the adjacent row.

5.3 The Board accept that this is an objective statement of the problem to be solved and that this problem is solved by the invention as claimed.

6. Inventive step

6.1 The Board can see no good reason why the skilled man, starting out from D1 and aware of the problems arising in this known arrangement, would so modify this known array as to provide a third emitter for each of the transistors of each memory cell and so arrange the array that a change in the potential of the first and third emitters from low to high is required in order to transfer data between transistors of adjacent rows. The Board can find no

teaching in D1 which would either suggest that a third emitter be provided or that the array be so arranged that the word line of each row goes from low to high in order to effect transfer. It would appear rather that the skilled man, faced with the technical problem to be solved, would seek to control carefully the voltage applied when the line goes low. Although the use of triple-emitter transistors is common general knowledge in the art, so that it might well be obvious to the skilled man that he could modify the D1 arrangement by providing such triple-emitter transistors if a further gate function were for any reason required, this does not lead to the conclusion that he would therefore provide a second word line and so arrange matters that both word lines must go high for transfer. The Board accordingly conclude that the subject-matter of Claim 1 involves an inventive step having regard to the disclosure of D1.

6.2 The Board has also found it necessary to address the question of whether the skilled man, aware of the disclosure of D2, would either be led by the teaching of this document, or would be led by it to modify D1, so as to arrive at the claimed invention. D2 discloses a memory array referred to as a "latent image memory", which combines some of the characteristics of ROM and random access memory. In the event of data corruption or loss a reset function is provided by means of hard-wiring of the power supply lines to the various cells so as to permit all the cells to be initialised simultaneously with basic data. Although at column 3, lines 46 to 50 of the description reference is made to use in a shift register, the only described embodiments are of a random access memory; the reference to a shift register is merely in the context of pre-setting the contents of each stage of a register as outlined above. Be that as it may, the Figure 1 embodiment uses triple-emitter transistors in

conjunction with two word lines (the "X" select and "Y" select lines); when both these lines are taken high an output can be derived. Although there is no specific teaching that the collectors of the transistors of a cell should be connected to emitters of the adjacent downstream transistors, as required by Claim 1, the skilled man would arguably be led in this direction by the passage at column 4, line 62 to column 5, line 6, indicating that when the word lines are taken high the output of a cell can be derived either from the collector voltages or from the data lines.

6.3 Although as indicated above D2 discusses how the content of a memory cell can be read by using the collectors, it does not appear to the Board to teach the manner in which the thus derived information can be passed to the next cell downstream, i.e. written into that cell. The reference to a "shift register" appears to be in the context of pre-setting the contents of each stage of the register as outlined above and there is no disclosure of rows and columns of memory cells so arranged as to pass data down the rows of a column of cells. Rather, the select lines are used to enable use of the array as a true random access memory.

6.4 The Board accordingly consider that the skilled man could not derive the claimed invention from D2 without the exercise of invention.

6.5 Nor do the Board consider that the skilled man, seeking to solve the problem in the D1 arrangement discussed above, would derive the solution from D2. As noted above, D2 relates to a "latent image" random access memory having "X" select and "Y" select lines so that each individual cell in the array can be addressed and can provide an output on data input/output lines shown in Figure 1 of D2

as lines "0" and "1". The Board accordingly consider that the skilled man would not seek an answer to his problem in the disclosure of D2.

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent on the basis of the Appellant's request (paragraph V above), with the errors noted in paragraph 3.2 above corrected.

The Registrar: The Chairman:

M. Beer P.K.J. van den Berg