BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS

BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE

CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

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File Number: T 141/91 - 3.5.1

Application No.: 86 108 812.8

Publication No.: 0 212 152

Title of invention: Microprocessor assisted memory to memory move apparatus

Classification: G06F 13/28

D E C I S I O N
of 12 August 1992

Applicant: HONEYWELL INC.

Headword:

EPC Article 56

Keyword: "Inventive step (yes) - unobvious replacement of units in known circuitry by new function of other units"

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number : T 141/91 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 12 August 1992

Appellant : HONEYWELL INC.
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Decision under appeal : Decision of Examining Division 2.2.01.065 of the European Patent Office dated 14 September 1990 refusing European patent application No. 86 108 812.8 pursuant to Article 97(1) EPC.

Composition of the Board :

Chairman : P.K.J. van den Berg
Members : W.B. Oettinger
F. Benussi

Summary of Facts and Submissions

I. The appeal lies against the decision of Examining Division 2.2.01.065, dated 14 September 1990, to refuse the European patent application 86 108 812.8, filed on 28 June 1986, on the ground that the subject-matter of Claim 1 of 9 July 1990, and of the dependent claims, lacks an inventive step, having regard to the following prior art documents:

D1: JP-A-59-72532,

D2: Wescon Conference Record, Vol. 25 (1981) September, El Segundo, CA (US), paper 3/1, pages 1-7.

In interpreting D1, the Examining Division relied in particular on:

D1a: the abstract of D1 in Patent Abstracts of Japan, Vol. 8 No 179 (17 August 1984)
D1t: an English translation of D1 filed by the Applicant.

II. More specifically, the Examining Division held that the characterising portion of said Claim 1 is not clear but if it is understood as the description suggests, a similar idea is used, in the context of the preamble of Claim 1, in D1(a,t), and that the only differences, which can be recognised, from this prior art are modifications which are to be considered as choices from a plurality of obvious alternatives, in particular when D2 is taken into consideration.

III. The appeal was lodged, and the respective fee paid, on 22 November 1990 with a request that the appealed decision be reversed and a patent granted.

On 24 January 1991, the Appellant filed a Statement of Grounds and, on 23 September 1991, an amended Claim 1 corresponding to a former auxiliary request.

IV. In the Statement of Grounds and in oral proceedings, held on 24 October 1991, the Appellant submitted, in support of an inventive step, that the claimed apparatus gives the data processing system a different and advantageous memory architecture with respect to D1. The claimed use of logic 52 and multiplexer 51 would be unique to the instant invention and result in an operation different from the prior art.

Of particular importance is the absence, in the claimed system circuitry, of NOP generator 5 and gate 9 of D1(a). Instead, the processor in the claimed apparatus is temporarily isolated from the data bus, over which DMA between the memory and the peripheral register is performed, by an interrupt routine including a dummy read command.

At the conclusion of the oral proceedings, the Board decided to offer the Appellant the opportunity to file new claims and an adapted description.

V. In response, the Appellant filed, on 20 December 1991, new claims and replacement pages. In reply to a Communication drawing attention to Rule 29(1) EPC, the Appellant replaced, on 3 July 1992, said claims.

The Appellant's request that a patent be granted is thus understood to include the following application documents:

- description, pages 1 and 2, filed on 20 December 1991,

pages 3 and 4, filed on 9 July 1990,
pages 5, 6 and 10 to 18, as published,
pages 7 to 9, filed on 9 March 1989;

- Claims 1 to 7, filed on 3 July 1992;

- drawing, sheet 1 to 3, as published.

Claim 1 reads as follows:

"Memory access control circuitry in a data processing system which includes:
- a memory (30) comprising a plurality of addressable locations (16 kBytes) for storing data in different memory modules (RAMs 30-1, 30-2, ROM 30-3),
- peripheral units (45) coupled to a peripheral controller (40) comprising a peripheral register (41) which subsequent to the issuance of a data request signal receives data read from said memory (30) and which subsequent to the issuance of a data ready signal transfers data for writing into said memory (30), said data request and data ready signals being generated by said peripheral controller (40) whenever occasion arises,
- a processor (10) capable of responding to the said data request and data ready signals whenever they are received from said peripheral controller (40),
- a bus (20) coupling together said memory, said peripheral controller (40) and said processor (10) for direct data transfer between the said units (10, 30, 40), said bus comprising
  - a data bus (22) for transferring the data between the said units (10, 30, 40), and
  - an address bus (21) for the transfer of address bits,

- a first subgroup (14) of the total available (16) address bits representing the address access bits (A_{13} -A_0) sufficient in number to access all of said memory locations (16 kBytes), and
- a second subgroup (2) of the total available (16) address bits representing the address control bits (A_{15}, A_{14}) for enabling direct transfer of data over said data bus (22),

- a control logic circuit (50) to enable the access to the data in said memory (30) and/or in said peripheral register (41), said control logic circuit comprising
  - a multiplexer (51) steering, under control of said address control bits (A_{15}, A_{14}), read/write signals (μP read and μP write strobe), supplied to its inputs (A0-3, B0-3, C0-3), to the units involved in said data transfer to effect reading and writing of said data from or into the accessed storage locations of said units involved and transferring said data over the data bus (22), and
  - address decoder means (52) responsive (at E of 53/54) to different configurations of said address control bits (A_{15}, A_{14}) to determine by this configuration the mode of data transfer between the units involved and to deliver, at output terminals (55, 56, 57) of the said address decoder means, output signals fed to the enable terminals (E of 30/41) of the memory modules and of the peripheral register to enable these to be operational and respond to the said read/write signals (RAM/ROM read, RAM write, peripheral read, peripheral write) delivered by said multiplexer (51), whereby
    - a first of said configurations of the said address control bits (A_{15}="1"; A_{14}="1") enables the processor (10) to access in a normal data transfer mode the memory (30) or the peripheral

register (41) for reading data therefrom or supplying data thereto,

- a second of said configurations of said address control bits (A_{15}="1"; A_{14}="0") effects direct memory access in a first direct access data transfer mode (MOVE PER ---> MEM) whereby data are transferred from said peripheral register (41) to said memory (30), and
- a third of said configurations of said address control bits (A_{15}="0"; A_{14}="1") effects direct memory access in a second direct access data transfer mode (MOVE MEM ---> PER) whereby data are transferred from said memory (30) to said peripheral register (41),

and whereby

- whenever the first configuration of said address control bits (A_{15}="1"; A_{14}="1") is valid, only one decoder means output terminal delivers an enable signal to the units (30-1 or 30-2 or 30-3 or 41) involved, and
- whenever the second or third configuration of said address control bits (A_{15}, A_{14} = "1 0" or "0 1") is valid, two decoder means output terminals deliver enable signals to the said units coupled thereto to effect direct transfer of data over said data bus (22) between the two units so enabled,

and whereby

- data transfer in the two direct access transfer modes is performed without resorting to an internal register of said processor (10),

c h a r a c t e r i z e d i n t h a t

the processor (10) in response to the receipt of the said data request or data ready signals performs an interrupt

routine (Fig. 6) which includes a read command (Overhead 2: "dummy read") by which

- a first set of address access bits (A_{11} - A_0) is applied to said address bus (21) to identify the storage locations in said memory (30) for data access, and a second set of at least two address access bits (A_{13}, A_{12}) is applied to the address decoder means (52) of the control logic circuit (50) to enable the access to the data in said memory (30) and/or in said peripheral register (41),
- the said address control bits (A_{15}, A_{14}) are applied to said address decoder means (52) of the control logic circuit (50) for the determination of the mode of data transfer between the units involved, and
- read and write strobe signals (μP read and μP write) are generated which are supplied to the inputs (A0-3, B0-3, C0-3) of the multiplexer (51) for their steering, under the control of the address control bits, to the units involved in said data transfer,

and further characterized in that

the said decoder means (52), in response to the second and third configurations of said address control bits (A_{15}, A_{14} = "1 0" or "0 1"), steers the said at least two address access bits (A_{13}, A_{12}), after their decoding (2:4), to the said decoder means output terminals in such different ways that

- whenever the second configuration of said address control bits (A_{15}, A_{14} = "1 0") is valid, two decoder means output terminals deliver enable signals to the respective units coupled thereto, and
- whenever the third configuration (A_{15}, A_{14} = "0 1") is valid, another pair of decoder means output terminals deliver enable signals to the respective units coupled thereto

to effect the direct transfer of data over said data bus (22) between the two units without disrupting the connective integrity of said data bus (22) with the processor (10)."

Claims 2 to 7 referring, either directly or indirectly, to Claim 1 are dependent claims.

Reasons for the Decision

1. The appeal is admissible (Articles 106 to 108 and Rule 64 EPC).

2. Disclosure

2.1 Claim 1 defines a memory access control circuitry in a data processing system - substantially more specifically than the original Claim 1 - in terms of the means it comprises and the functions these means perform.

2.2 All of said means can be found in the drawings representing a preferred embodiment of the claimed circuitry:

- Fig. 1 shows the whole system with the memory (30), one peripheral unit (45) with controller (40) including register (41), the processor (10), the bus (20), and their connections;

- Fig. 3 shows the memory (30) modules (RAM1 30-1, RAM2 30-2, ROM 30-3), again the peripheral register (41), the bus (20) address (21), data (22) and control (e.g. A_{15}) lines, the control logic (50), and their connections;

- Fig. 4A shows the multiplexer (51) comprised in the control logic (50); and

- Fig. 5 shows the enable logic (52) comprised in the control logic (50) including 2:4 decoders, again the memory (30) modules (-1, -2, -3) and the peripheral register (41), and their connections.

2.3 Their functions can be derived from the description of these means with reference to Figures 3, 4A and 5 and from the description relating to logic diagram Fig. 4B.

2.4 It is noted that Claim 1 does not, as did the original Claim 1, expressly specify the memory modules as "corresponding to an assigned area of a first memory map, ... duplicated into a plurality of mirrored memory maps, each ... corresponding to a predefined operation, ...".

The omission of this statement from the Claim 1 rejected by the Examining Division was not, however, objected to by the Division, and the Board agrees that the omitted statement does not constitute a technical feature which would be necessary, beyond the definitions given in Claim 1, to define the matter to be protected.

2.5 Hence, by the amendments made to Claim 1, this claim does not introduce any subject-matter extending beyond the content of the application as originally filed (Article 123(2) EPC).

2.6 The dependent claims define additional features, including functions, of the claimed means of a preferred embodiment of the claimed circuitry, these features, or functions, being derivable from the description of that embodiment.

3. Clarity and partitioning of Claim 1

3.1 The decision under appeal is based on the silent assumption that - in contrast to the original Claim 1 - the rejected Claim 1 was clear, and in the Board's opinion this is true also for Claim 1 now on file (Article 84 EPC).

3.2 Claim 1 is partitioned in accordance with Rule 29(1)(a) and (b) EPC, in view of the prior art coming nearest to the claimed invention, this prior art being represented by D1(a,t).

In his latest response, the Appellant has submitted that the function of the claimed decoder means (52) is so different from that of the decoder (7) of D1(a), and the function of the claimed multiplexer (51) is so different from that of the multiplexer (10) of D1(a), that some of the functional features included in the precharacterising portion of Claim 1 might not in effect be known in the context of these means from D1(a). The only reason why the Appellant does not propose Claim 1 to be amended one more time is that the Board has indicated its intention to decide the appeal case without any further exchange of opinions.

Indeed, in the opinion of the Board, in the present state of affairs, and on the basis of the file history, it is not certain that the Board would have given its consent under Rule 86(3), second sentence, EPC to another amendment unless this amendment would have been clearly allowable and appropriate.

Nevertheless, the Board has checked whether, on the basis of the Appellant's latest submissions, Claim 1's partitioning would appear to be clearly wrong. This is not the case for the following reasons:

It is certainly true that the function of the decoder means and the function of the multiplexer in both cases, D1 and the application, is different. But, in the opinion of the Board, this has been taken into account in present Claim 1.

It is, for instance, absolutely true that the address control bits on which the multiplexer works in both cases, are not the same: they are A_{13} in D1 but A_{15}/A_{14} in the application. But this fact does not have for its consequence that the "multiplexer" feature cannot be read on D1. In D1, A_{13} must be regarded as belonging to the control bits defined in the "second subgroup" feature (i.e. not to the access bits defined in the "first subgroup" feature). On this understanding, the "multiplexer" feature can well be read on D1 (with "control bits" read as including A_{13}).

Similarly, the wording of the "address decoder means ..." feature does not seem to be factually incorrect or not applicable to D1. Specifically the recited passage "whenever the second or third configuration ... is valid ..." does not necessarily define two different configurations in the prior art transfer control; rather it may be construed as only indicating that this feature applies to both transfer directions, viz. to both the "second configuration" feature and the "third configuration" feature defined in the preamble. When read on D1, the "second" and "third" configuration in the "whenever" feature must, therefore, be understood as being one and the same configuration. For the claimed invention, this is different, but this will be made clear by the "whenever" features in the characterising portion of the claim, in particular by the word "another".

While it would perhaps be possible to find a wording for Claim 1 fitting the prior art situation even better, the Board considers the present wording sufficiently clear in respect of its prior art portion.

3.3 Therefore, the Board considers it appropriate to decide the issue of the appeal without any further procedural action preceding.

4. Patentability

In the circumstances, there is no other issue to be decided than the question of inventive step (Article 56 EPC), the other requirements for patentability (Article 52(1) EPC), such as novelty (Article 54 EPC), being clearly met without this requiring any further reasoning.

4.1 As stated (paragraph 3.2), all the means (paragraph 2.2) mentioned in the preamble of Claim 1 (refer to paragraph V) are to be regarded as known from D1 (interpreted by D1t) and/or D1a.

The same applies to their connections and to their functions as far as these functions have been defined, somewhat generally, in the preamble. This applies, even, to the "control logic circuit" comprising a "multiplexer" (10) and "address decoder means" (7), to their connections with the processor (1) and with the memory (2, 3) and peripheral unit (4) via bus (a, b) and (other) control lines, and to their general function of enabling, in dependence upon different control bit configurations, normal data transfer or direct memory access in either of both directions.

As a particular point, it is noted that direct access transfer is performed in the circuitry of D1 and D1a, as

it is in the claimed circuitry, without resorting to an internal register of the processor.

4.2 For the implementation of the direct transfer of data between a memory (3) and the peripheral controller (4), the circuitry of D1 and D1a has, in addition to the aforementioned means, an NOP (generally understood as "no operation") generator (5) and a gate (9) separating, in the direct transfer modes, the data bus portions connecting the memory (3) and the peripheral controller (4) from the remaining portions of the data bus (b).

One, although a negative, feature distinguishing the claimed circuitry from the one of D1(a) is the absence of the NOP generator and of the bus gate.

This absence is, however, indicated in Claim 1 by the statement that direct transfer is effected without disrupting the connective integrity of the bus with the processor.

4.3 The positive features distinguishing the claimed circuitry from the one known from D1(a) must be seen in the functions of the circuits as they are defined, more specifically than the general functions in the preamble, in the characterising portion of Claim 1 (refer to paragraph V).

In particular, during direct memory access, according to the claimed invention the circuits not involved in the direct access are separated from those involved in the direct access by the processor performing an interrupt routine including a dummy read command, this function of the processor replacing the function of the gate (9) and of the NOP generator (5) of D1(a).

4.4 Other differences between the known and the claimed circuitries are to be seen in the following details:

In D1(a), the memory consists of a ROM (2), not involved in direct memory access, and a RAM (3) taking part in the direct memory access. Direct transfer of data is always (in either one of both directions) between this (single) RAM and the peripheral controller. The peripheral controller is enabled by an I/OCS signal and the RAM by a RAMCS signal from the address decoder (7). Whenever also the NOP generator (5) is activated (NOPCS) and the gate (9) closed, the multiplexer (10) selects A13 instead of R/W (read/write) for enabling the units involved (3, 4).

In the claimed invention, the memory consists of a ROM (30-3), not involved in direct memory access, and of two RAM modules (30-1, 30-2) taking part in the direct memory access. Direct transfer of data can be accomplished between either one of said two RAM modules and the peripheral register (also in either one of both directions).

Although Claim 1 does not explicitly state that there are two RAM modules, these differences in detail are implied in its characterising portion in the "whenever" features, for instance by the term "another pair ...".

4.5 The aforementioned features distinguishing the claimed circuitry positively from D1 (paragraph 4.3), in combination with the implied negative features (paragraph 4.2), are clearly not suggested in D1 (D1t) or D1a.

Although there is a reference in D1t to an interrupt signal (IRQ), it follows from the functions of the NOP generator and of the bus gate (9), in particular its "separating" function (cf. paragraph 4.2), that it is not

the function of the processor to perform, as claimed in the first characterising feature of Claim 1, in response to data request or ready signals an interrupt routine including a dummy read command.

4.6 Nor can a suggestion to this effect be found in D2.

The statement (page 1, last paragraph), made in the context of data transfer between a RAM and a co-processor, that the data are ignored by the host processor does not, in the absence of any further information, appear to be sufficiently specific for giving the skilled person an incentive to replace the NOP generator and the bus gate of D1 by an interrupt routine of the processor including a dummy read command.

4.7 In these circumstances, it is of no relevance whether or not the additional details distinguishing Claim 1 from D1(a) (paragraph 4.4) contribute anything to the unobviousness of the claimed circuitry.

Rather, the aforementioned reasons (paragraph 4.5 and 4.6) are sufficient for concluding that the subject-matter of Claim 1, and consequently of all claims on file, involves an inventive step.

5. Conclusions

The claims on file are, therefore, allowable.

No objection arises in respect of the other application documents on file (cf. paragraph V).

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance department with the order to grant a patent on the basis of the application documents mentioned in paragraph V.

The Registrar: The Chairman:

M. Kiehl P.K.J. van den Berg