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- timing means for precisely measuring the time duration of one or more cycles of said wheel signal, said means comprising themselves clock means (13) for generating a periodic clock signal - to wit, the "reference pulses (22)" - first counter means (10) for counting clock signal cycles and second counter means (8) for counting wheel signal cycles - see column 2, lines 46 to 51 and column 3, lines 8 to 11;

- digital control means (11) arranged to provide an enabling signal - see column 2, lines 41 to 46 - and

- gating means (9, 7) for selectively enabling the first and second counter means (10, 8), said gating means having a first input receiving said enabling signal from said digital control means (11) and a second input receiving the signal (6) from said wheel signal generating means (2, 3) - see column 2, lines 41 to 46 again and Figure 4.

The AC wheel signal (4) supplied by the electromagnetic pick-up (3) is shaped into a rectangular pulse train (6) by shaping circuit (5) before being applied to the input terminal of the gate (7) and to the clock input terminal of a flip-flop (12) - see column 2, lines 38 to 41. The signal enabling the gates (7) and (9) to start a counting cycle is produced by the flip-flop (12) in response to the first signal of the pulse train (6) which appears after the disappearance of a signal (21) applied from a gate (11) - see column 2, lines 41 to 46. The variations of a square signal, however, are discontinuous and, therefore, occur at times which are related to a determined phase angle of the continuous signal from which said square signal is derived. It may thus be accepted that, in the device known from (D1), the timing means comprise means (12) responsive to a predetermined phase angle of the

BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS

BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE

CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

A		B		C	X

File Number: T 313/91 - 3.4.1

Application No.: 80 303 353.9

Publication No.: 0 026 636

Title of invention: Digital wheel speed sensor

Classification: B60T 8/32

D E C I S I O N
of 6 August 1992

Proprietor of the patent: Crane Co.

Opponent: Siemens Aktiengesellschaft, Berlin und München

Headword:

EPC Article 56

Keyword: "Inventive step (no)"

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number : T 313/91 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 6 August 1992

Appellant : (Proprietor of the patent)	Crane Co. 300 Park Avenue New York New York 10022 (US)
Representative :	Cross, Rupert Edward Blount Boult, Wade & Tennant 27 Furnival Street London EC4A 1PQ (GB)
Respondent : (Opponent)	Siemens Aktiengesellschaft, Berlin und München Postfach 22 16 34 W-8000 München 22 (DE)
Representative :	Zelenka, Hermann Siemens Aktiengesellschaft
Decision under appeal :	**Decision of Opposition Division of the European Patent Office dated 18 February 1991 revoking European patent No. 0 026 636 pursuant to Article 102(1) EPC.**

Composition of the Board :

Chairman : G.D. Paterson
Members : Y. van Henden
H.J. Reich

Summary of Facts and Submissions

I. The Appellant is owner of European patent No. 0 026 636.

II. The patent was opposed by the Respondent on the grounds mentioned in Article 100(a) EPC, referring inter alia to the prior art which can be derived from documents

D1: US-A-3 757 167

D2: SAE Paper 75/0432, pages 65 to 74, T.O. Jones et al., "Application of Microprocessors to the Automobile", April 1975.

III. The Opposition Division revoked the patent.

IV. The Appellant lodged an appeal against this decision. He requested said decision to be set aside and the patent to be maintained as granted.

Subsidiarily, he requested maintenance of the patent in amended form on the basis of a new set of claims submitted with his statement of grounds of appeal and, if the Board were intending not to allow the appeal, the appointment of oral proceedings.

V. In a communication pursuant to Article 11(2) of the RPBA, the Board took the provisional view that, with regard to the state of the art revealed i.a. by documents (D1) and (D2), none of the claims forming the basis of the Appellant's main and auxiliary request involved an inventive step.

VI. With his comments on the Board's communication, the Appellant submitted on 2 July 1992 two sets of claims to be examined at the oral proceedings, the first set comprising four claims and forming the basis of his main

request, and the second set forming the basis of an auxiliary request comprising nine claims, those numbered 1, 5 and 7 being independent ones.

VII. Claim 1 according to the Appellant's main request reads:

"A brake control system including a rotatable wheel; wheel signal generating means (20, 40) which produces a periodic wheel signal having a frequency indicative of the rate of rotation of the wheel; and timing means for precisely measuring the time duration of one or more cycles of said wheel signal and comprising clock means (240) for generating a periodic clock signal, first counter means (470) for maintaining a count of clock signal cycles, second counter means (450) for maintaining a count of wheel signal cycles, gating means (490) for selectively enabling and disabling the first and second counter means and digital control means arranged to provide an enabling signal having a period independent of the frequency of the wheel signals, said gating means having a first input receiving said enabling signal from said digital control means and a second input from said wheel signal generating means, and incorporating means responsive to a predetermined phase angle of said wheel signal for controlling the gating means to enable the first and second counter means at the first occurrence of said phase angle following said enabling signal from said digital control means and to disable the first and second counter means at the first occurrence of said phase angle following the removal of the enabling signal, whereby said second counter contains a count of an exact number of cycles of the wheel signal while said first counter contains a count of clock signals corresponding to the elapsed time during said number of cycles; characterised in that said digital control means is a microprocessor subsystem arranged

a) to generate and remove said enabling signal,

b) to read and store said counts after the first and second counters have been disabled,

c) to calculate from said stored counts a value for wheel speed or the period of said wheel signal, and

d) to produce a control signal for anti-skid brake control."

Claims 2 to 4 are appended to Claim 1.

Independent Claims 1, 5 and 7 of the Appellant's auxiliary request have the same pre-characterising clause as Claim 1 of the main request, except that, in Claim 5, a comma was deleted after "a second input from said wheel signal generating means", whereas additional commas were inserted after "disabling the first and second counter means" and after "following said enabling signal from said digital control means". The characterising part of Claim 1 reads:

"...; characterised in that said digital control means is a microprocessor subsystem having means generating periodic clock controlled interrupt signals to pace the execution of the microprocessor program, the subsystem being arranged

a) to generate and remove said enabling signal in response to said interrupt signals, ..."

(same combination as in Claim 1 according to the Appellant's main request).

The characterising part of independent Claim 5 according to the auxiliary request reads:

"...; characterised in that the system includes a further rotable wheel with respective further said wheel signal generating means, first and second counter means and gating means, and in that said digital control means is a microprocessor subsystem arranged

a) to generate and remove respective said enabling signals for the gating means of each of said wheels,

b) to read and store respective said counts when the first and second counters of the respective wheels have been disabled,

c) to calculate from said stored counts values for the speeds of the respective wheels or for the periods of the respective wheel signals, and

d) to produce control signals for anti-skid brake control,"

a minor clerical error being here corrected.

The characterising part of independent Claim 7 according to the auxiliary request reads:

"...; characterised in that said digital control means is a microprocessor subsystem arranged

a) to read and store the counts stored in the first and second counter means (470, 450) at a first time;

b) to provide the enabling signal at a second time, subsequent to the first time, to cause the gating means

(490) to enable the first counter means (470) at the next occurrence of the predetermined phase angle of the wheel signal;

c) to remove the enabling signal at a third time, subsequent to the second time, to cause the gating means (490) to disable the first counter means (470) at the next occurrence of the predetermined phase angle of the wheel signal;

d) to read and store the counts stored in the first and second counter means (470), 450) at a fourth time, subsequent to the third time and after the first counter means (470) has been disabled;

e) to calculate the difference between the count stored in the first counter means (470) at the first and fourth times as a measure of elapsed time;

f) to calculate the difference between the count stored in the second counter means (450) at the first and fourth times as a measure of the number of wheel signal cycles occurring during the elapsed time;

g) to calculate from said differences a value for wheel speed or the period of said wheel signal; and

h) to produce a control signal for anti-skid brake control."

Claims 2 to 4 of the auxiliary request are appended to Claim 1, Claim 6 is appended to Claim 5 and Claims 8 and 9 are appended to Claim 7.

VIII. Oral proceedings were held on 6 August 1992.

IX. In support of his requests, the Appellant substantially argued as follows:

The inventive concept resides not simply in the use of a microprocessor but in the manner of using the latter. At the priority date of the patent, microprocessors were still fairly new and, as evidenced by (D2), many people were speculating on what could be done with them. As a matter of fact, (D2) only says that a microprocessor can read prepared digital input data such as wheel speed data, manipulate said data according to a desired algorithm, and output a digital control signal, for instance a wheel lock control signal. Nevertheless, (D2) does not suggest to arrange the microprocessor in such a way that it generates and removes an enabling signal for controlling the operation of the counters, nor to make it read and store the counts after said counters have been disabled in order that it generates the wheel speed signal. There is also no suggestion in (D2) that, with microprocessors, a reduction in size, cost and power dissipation might be expected in comparison with prior art.

It is now clear that a plurality of intermediary measures are needed to incorporate a microprocessor in the circuit known from (D1). Bearing in mind the teachings of (D2), it may be supposed that a skilled person would have used the microprocessor to read the contents of counters (8,10) and calculate the wheel speed. For starting the operation of the microprocessor, he would have envisaged the application of a signal generated by the wheel speed sensor circuitry, for instance an input signal derived from the flip-flop (12). This, however, would have required an interruption of other operations being performed and, therefore, would have been detrimental to efficiency.

According to the invention, the microprocessor generates an enabling signal having a period independent of the wheel signal frequency. It thus determines when a fresh count will be available and operates always with the freshest data. Thereby, the brake control signal can be more closely tied (in time) to the current status of the wheel than it is with the device known from (D1), where the division must be made before starting the next measure, or with a device embodying the teachings of (D2), where at least two successive readings are necessary to cancel the consequences of the error made on the count of wheel signal pulses. This advantage is of decisive importance in a brake control system specially designed for the aircraft industry, i.e. having to meet much more severe requirements than those of the automotive industry.

X. The Respondent's argumentation may be summarised as follows:

Document (D2) reveals that the utilisation of computers in brake control systems for cars was known before the priority date of the patent, as well as the interest of replacing them by microprocessors. Therefore, starting from the prior art disclosed in (D1), no display of inventiveness was required to arrive at the invention.

With respect to the disclosure in (D1), the essential difference of the claimed brake control system is that it comprises a microprocessor which, according to the patent application as filed, may belong to the Z80 family of the firm Zilog, Inc., and is so programmed that it carries out the known process. This, however, is nothing other than the use for which microprocessors have been designed and, from the "Technical Manual" referred to in the patent

application, the skilled person could learn how to wire and program them. Said manual was copyrighted by Zilog, Inc. two years before the priority date of the patent but, anyway, it was already known that microprocessors are smaller and faster than computers and, since 1975, they also are cheaper.

The Appellant's contention that (D2) would only suggest to replace by a microprocessor the dividing circuit (16) of the wheel speed measuring system described in (D1) is not relevant. Figure 8 of (D2) refers indeed to an anti-skid system in which a microprocessor reads and stores the contents of counters before dividing. Said microprocessor is of the kind described with reference to Figure 4 and substantially comprises the same constituent units as the one to be used according to the patent in suit. Likewise, whether the requirements of the aircraft industry are more severe than those of the automotive industry does not matter, for the claimed subject-matter is a wheel speed measuring device rather than an anti-skid control system for aircraft. Besides, said requirements can be met by working at a higher frequency and, in 1969, working frequencies could already be as high as 5 MHz, i.e. the double of what is needed here. Finally, measuring the speeds of a plurality of wheels is also envisaged in (D2).

XI. At the end of the hearing, the Chairman announced the decision that the appeal was dismissed.

Reasons for the Decision

1. Definition of the matter for which protection is sought.

According to the pre-characterising clause of each independent claim submitted as basis of the Appellant's requests, the counter means (470, 450) are said to be provided for maintaining a count of "clock signal cycles" and of "wheel signal cycles", respectively. The Board, therefore, interprets the last statement of said clause as meaning that "the first counter contains a count of clock signal cycles corresponding to the elapsed time during said number of cycles" (of the wheel signal).

In the Board's judgment, it must also be understood that the gating means (490) has "a second input receiving the periodic wheel signal from the wheel signal generating means (20, 40)" rather than "a second input from the wheel signal generating means".

The Appellant did not dispute this interpretation of the claims.

2. Novelty

2.1 Keeping the terminology of Claim 1 according to the Appellant's main request, the "revolution measuring instrument" described in document (D1) comprises:

- a rotatable wheel (1);

- wheel signal generating means - namely: the gear (2) mounted on the wheel (1) and the electromagnetic pick-up (3) - which produce a periodic wheel signal having a frequency indicative of the rate of rotation of the wheel - see column 2, lines 35 to 38 and Figure 4;

signal cycles and second counter means (8) for counting wheel signal cycles - see column 2, lines 46 to 51 and column 3, lines 8 to 11;

- digital control means (11) arranged to provide an enabling signal - see column 2, lines 41 to 46 - and

- gating means (9, 7) for selectively enabling the first and second counter means (10, 8), said gating means having a first input receiving said enabling signal from said digital control means (11) and a second input receiving the signal (6) from said wheel signal generating means (2, 3) - see column 2, lines 41 to 46 again and Figure 4.

The AC wheel signal (4) supplied by the electromagnetic pick-up (3) is shaped into a rectangular pulse train (6) by shaping circuit (5) before being applied to the input terminal of the gate (7) and to the clock input terminal of a flip-flop (12) - see column 2, lines 38 to 41. The signal enabling the gates (7) and (9) to start a counting cycle is produced by the flip-flop (12) in response to the first signal of the pulse train (6) which appears after the disappearance of a signal (21) applied from a gate (11) - see column 2, lines 41 to 46. The variations of a square signal, however, are discontinuous and, therefore, occur at times which are related to a determined phase angle of the continuous signal from which said square signal is derived. It may thus be accepted that, in the device known from (D1), the timing means comprise means (12) responsive to a predetermined phase angle of the wheel signal to enable the first and second counter means (10, 8) at the first occurrence of said phase angle following the enabling signal - namely the zero level of signal (21) - from the digital control means (11). The

wheel signal to enable the first and second counter means (10, 8) at the first occurrence of said phase angle following the enabling signal - namely the zero level of signal (21) - from the digital control means (11). The first counting means (10) is obviously disabled at the first occurrence of the predetermined phase angle following the removal of the enabling signal, since time pulses are counted from the first to the (n+1)th wheel signal pulse - see column 2, lines 22 to 30. Nevertheless, the same cannot be asserted with absolute certitude with respect to the second counting means (8). It is indeed stated in the latter passage of (D1) that (n) is the number of wheel signal pulses appearing within the time period (To) - which in most cases is shorter than (n) periods of the wheel signal - and Figure 3 shows that the wheel signal pulse initiating said period (To) is counted as the first one. From these teachings, it can be inferred that the second counter (8) is disabled after the time (To) has elapsed and before the occurrence of the (n+1)th wheel signal pulse, i.e. within a time interval during which the phase angle of the wheel signal is different from the predetermined value. When the counter means are disabled, the second one contains a count of a number of cycles of the wheel signal, whereas the first one contains a count of clock signals corresponding to the elapsed time during said number of cycles. Finally, a control signal for anti-skid brake control is produced.

2.2 Document (D1) teaches that the signal (21) disappears on completion of the dividing operation, and that the latter is performed during a time interval of duration (Tp) starting from the (n+1)th pulse of the wheel signal -see: Figure 6; column 2, lines 11 to 23; column 4, lines 60 to 63. With the measuring instrument known from (D1), the period of the enabling signal thus appears to be a whole

multiple of the period of the wheel signal. The period of the enabling signal, therefore, is not absolutely independent of the wheel signal frequency.

2.3 With regard to the prior art disclosed in (D1), the subject-matter of Claim 1 according to the Appellant's main request is novel in that

- the enabling signal provided by the digital control means has a period independent of the frequency of the wheel signal;

- the second counter means is disabled at the first occurrence of the predetermined phase angle following the removal of the enabling signal, and in that

- the digital control means is a microprocessor subsystem arranged to generate and remove said enabling signal, to read and store the counts of clock signal cycles and wheel signal cycles after the counters have been disabled and to calculate from the stored counts the wheel speed or the period of the wheel signal.

2.4 The subject-matter of Claim 1 according to the Appellant's auxiliary request is furthermore distinguished over the prior art achievement of (D1) in that the microprocessor subsystem "has means generating periodic clock controlled interrupt signals to pace the execution of the microprocessor program", and in that the enabling signal is generated and removed "in response to said interrupt signals".

2.5 The subject-matter of Claim 5 according to the Appellant's auxiliary request is distinguished over the disclosure of (D1) by the same features as that of Claim 1 according to the Appellant's main request, in that it includes a

further rotatable wheel with related first counter means, second counter means and gating means, and in that the microprocessor is arranged to drive these further counter means and gating means in the same manner as those related to the first wheel to calculate the speed of the further wheel or the period of the corresponding wheel signal.

2.6 The subject-matter of Claim 7 according to the Appellant's auxiliary request is distinguished over the disclosure of (D1) in that the period of the enabling signal is independent of the wheel signal period, the second counter means is disabled at the first occurrence of the predetermined phase angle following the removal of the enabling signal, and in that the digital control means is a microprocessor subsystem arranged to carry out the steps (a) to (g) mentioned in the characterising part of the claim.

3. Inventive step

3.1 While slowing down a vehicle, wheel skid is liable to occur at every moment. Therefore, if a digital control system is used, no reliable skid prevention would be provided if the wheel rotation speed were not measured at time intervals sufficiently near to one another. Now, if a given time interval separating successive wheel speed determinations is sufficiently short to provide a reliable control at the maximum speed of a vehicle, determining the wheel speed at times separated by the same interval will also provide a reliable control at any lower speed of said vehicle. With regard thereto, however, no inventive step can be perceived in outputting an enabling signal which has a period independent of the vehicle speed and, consequently, independent of the wheel signal frequency.

As a matter of fact, if (n) is assumed to be sufficiently large, the latter condition is nearly met in the apparatus known from (D1). The time (To) is indeed a predetermined one - see column 2, lines 22 to 24 - and, from Figure 6, it appears that it is comprised between (n-1) and (n) periods of the wheel signal. The period of the enabling signal being (n+1) times that of the wheel signal, it thus exceeds (To) at most by twice the period of the wheel signal. Therefore, if (n) is large enough, the variation of the enabling period may be disregarded. The Appellant actually did not contest that, nor that it lies within the normal range of capability of the skilled person to envisage disabling both counter means (10, 8) simultaneously, i.e. at the first occurrence of the predetermined phase angle following the removal of the enabling signal.

3.2 In the embodiment of the invention described in relation with Figures 2 and 2A of the patent in suit, the microprocessor subsystem includes a Z80-CPU (600), two RAM chips (570, 580), a ROM chip (590) and a Z80-PIO chip (610) - see page 4, lines 50 and 51, corresponding to lines 18 to 20 of page 23 in the related patent application. The latter, however, reveals that the Z80-PIO interface circuit and the Z80-CPU are described in technical manuals copyrighted by the manufacturer, to wit Zilog, Inc., in 1977 - see page 9, lines 11 to 16, and page 13, lines 1 to 6. The application as filed also reveals that the Z80-CTC programmable counter circuit is described in a product specification of Zilog, Inc. dated October 1977 - see page 12, lines 3 to 7 and note that the counters (452-1) and (452-2) of Figure 2 are such circuits.

With regard thereto, the Board does not accept the Appellant's submission that, at the priority data of the

patent in suit, i.e. about two years after said technical manuals or product specification had been made available to the public, people skilled in the art would have been speculating on what could be done with microprocessors. As a matter of fact, this submission is belied by the still older document (D2), which envisages the use of microprocessors in brake control systems - see pages 72 and 73, section headed "wheel lock control" - and, anyway, it is hardly believable that the chip industry would invest money in the development of new components without previously inquiring about the need or the potential demand for such components.

3.3 Document (D2) reveals that, more than four years before the priority date of the patent in suit, the feasibility of performing various automotive functions using the technology of microprocessors was investigated. Besides the advantages which digital systems were already known to exhibit over analog systems, a reduction in size, cost and power dissipation was expected from the use of microprocessors - see page 65, first two paragraphs of "Introduction", and page 66, section headed "Digitizing the analog functions"; see also page 1 of the patent in suit, lines 13 to 25, from which it appears that the present invention too aimed at a change from analog to digital in order to improve brake control systems.

It is true that, as the Appellant put forward, size, cost and power dissipation are said in (D2) to be reduced in comparison to the corresponding values involved by the use of computers. Nevertheless, in 1975, the skilled person did not ignore that size and power dissipation of integrated circuits are much smaller than those of any equivalent conventional circuit. Therefore, as actually evidenced by the content of (D2), an incentive to extend the use of microprocessors to brake control systems was given to the skilled person.

The Appellant furthermore drew attention to the so-called "truncation error cancellation" mentioned in (D2) in relation with the determination of wheel speed - see the section headed "Error analysis" and Figure 1. It must nonetheless be taken into account that anti-skid brake control is there only one among a plurality of tasks laid down on the system - see "Abstract", where the functions performed by said system are listed. Moreover, document (D2) mentions that the system should include functions which require relatively high resolution and accuracy, as well as functions which require considerable data tabulation and storage - see the paragraph bridging pages 65 and 66. Therefore, it was clear to the skilled person reading (D2) that, where only wheel speed has to be measured, eliminating the truncation error by counting clock signal cycles during a whole number of wheel signal cycles, as disclosed in (D1), did not exceed the computational capacity of a microprocessor.

3.4 The microprocessor referred to in (D2) comprises a central processing unit (CPU), timing circuits, input and output interfaces, a random access memory (RAM) for storing temporary data used in the course of computations and a programmable read only memory (PROM) used to store the actual program steps - see Figure 4 and section headed "MOS Microprocessor". Speed being one of the parameters to be controlled by the system described in (D2), it is thus clear that the microprocessor subsystem referred to there is arranged to read and store counts of clock signal cycles and wheel signal cycles in the RAM of its memory, and to calculate from the stored counts the wheel speed or the period of the wheel signal. The Board, therefore, concurs with the Respondent as regards this point. Now, bearing in mind that the program steps are stored in the PROM of the microprocessor, it is obvious that the latter is also the unit deciding when counts will be started and

stopped, i.e. that said microprocessor generates and removes an "enabling signal" which, either alone or in conjunction with the generation of appropriate sensor and/or timing signals, determines the times at which the counts are started and stopped, respectively.

In the Board's judgment, therefore, no exercise of inventive ingenuity was required from the skilled person to envisage, before the priority data of the patent in suit, the use of a microprocessor in place of the units which, in a circuit according to Figure 4 of (D1), determine the sequence of steps to be performed. The Board furthermore observes that, contrary to the Appellant's submissions, said units are not limited to the dividing circuit (16) but also include the gates (9, 14), the counter (15) and the flip-flop (22). It is thus excluded that the skilled person would have proceeded as the Appellant contends, in particular that he would have envisaged to start the operation of the microprocessor through the application of a signal generated by the wheel speed sensor circuitry. Finally, no inventive step can be perceived in the independence of the enabling signal period with respect to the wheel signal frequency. This latter feature is indeed related to the desired rate of wheel speed determinations but, either alone or in combination with other measures featuring the invention, it does not provide any unexpected advantageous result.

3.5 In the Board's judgment, therefore, Claim 1 according to the Appellant's main request lacks an inventive step.

3.6 Claim 1 according to the Appellant's auxiliary request also lacks an inventive step, since means generating periodic clock controlled interrupt signals to pace the execution of the program are obviously necessary and, anyway, provided in the device known from (D1) - see

section 2.1 of the present decision - and in the microprocessor subsystem known from (D2) - see Figure 4 and section headed "Hardware configuration".

3.7 Controlling the respective speeds of a plurality of wheels is envisaged in (D2) - see the first sentence of the section headed "Wheel Lock Control". Knowing, however, that microprocessors are fast and have a high computational capacity, no reason was liable to deter the skilled person from providing for each wheel respective wheel signal generating means, respective first and second counter means and respective gating means, nor from elaborating an algorithm such that respective enabling signals for the gating means be generated, that respective counts of clock signal cycles and wheel signal cycles be read and stored in the memory after the counters have been disabled, and that the respective wheel speeds be calculated from the stored count values. Therefore, in the Board's judgment, Claim 5 according to the Appellant's auxiliary request also lacks an inventive step.

3.8 If signal cycles are to be counted only when a wheel speed measurement is being carried out - which is at the discretion of the programmer - then it is an obvious necessity first of all to read and store the initial counts before starting a measuring operation, hence before providing the signal enabling the means counting the clock signal cycles and wheel signal cycles - cf. clauses (a) and (b) of Claim 7 according to the Appellant's auxiliary request. It is likewise obvious that any signal can only be removed after it has been generated - cf. clause (c) - and, since the wheel speed can only be calculated from the variations of the counts of clock signal cycles and wheel signal cycles, it is also obvious to read and store the new counts, then to calculate the differences between said new counts and the respective initial ones, and then to

calculate from said differences the wheel speed value or wheel signal period before producing a control signal for anti-skid brake control.

There being no possibility of changing the order of the steps recited in the characterising part of Claim 7 according to the Appellant's auxiliary request, the latter claim too lacks, in the Board's judgment, an inventive step.

4. None of the independent claims on which the Appellant's main and auxiliary request are based is allowable - Article 52(1) EPC in relation to Article 56 EPC.

Order

For these reasons, it is decided that:

The appeal is dismissed.

The Registrar: **The Chairman:**

M. Beer **G.D. Paterson**